

ADVANCED SATELLITE COMMUNICATION SYSTEM

FINAL REPORT

SBIR 1988 Phase II

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Submitted By:
Amerasia Technology, Inc.
2248 Hampshire Road
Westlake Village, CA 91361

Principal Investigators
Dr. Edward J. Staples
Mr. Sen Lie

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PROJECT SUMMARY

The objective of this research program was to develop an innovative advanced satellite receiver/demodulator utilizing surface acoustic wave (SAW) chirp transform processor and coherent BPSK demodulation. The algorithm of this SAW chirp Fourier transformer is of the Convolve-Multiply-Convolve (CMC) type, utilizing off-the-shelf reflective array compressor (RAC) chirp filters. This satellite receiver, if fully developed, was intended to be used as an on-board multichannel communications repeater.

The Advanced Communications Receiver consists of four units --(1) CMC processor, (2) single sideband modulator, (3) demodulator, (4) chirp waveform generator and individual channel processors. The input signal is composed of multiple user transmission frequencies operating independently from remotely located ground terminals. This signal is Fourier transformed by the CMC Processor into a unique time slot for each user frequency. The CMC processor is driven by a waveform generator through a single sideband (SSB) modulator. The output of the coherent demodulator is composed of positive and negative pulses, which are the envelopes of the chirp transform processor output. These pulses correspond to the data symbols. Following the demodulator, a logic circuit reconstructs the pulses into data, which are subsequently differentially decoded to form the transmitted data.

The coherent demodulation and detection of BPSK signals derived from a CMC chirp transform processor were experimentally demonstrated and bit error rate (BER) testing was performed. To assess the feasibility of such advanced receiver, the results were compared with the theoretical analysis and plotted for an average BER as a function of signal-to-noise ratio.

Another goal of this SBIR program was the development of a commercial product. The commercial product developed was an *arbitrary waveform generator*. The successful sales have begun with the delivery of the first arbitrary waveform generator.

1.0 PHASE II OBJECTIVES

The objective of the Phase II program effort includes the design, fabrication, testing and documentation of an Advanced Satellite Receiver/Demodulator using an innovative transform processor and coherent QPSK demodulator. However, due to unexpected technical problems coupled with time and funding constraints a coherent BPSK Demodulator was developed. The Phase II program will demonstrate, evaluate, and characterize a receiver/BPSK demodulator as a proof of concept system for satellite communications. The processor will demonstrate the chirp transform technique for optimally receiving and decoding transmissions from many systems users.

2.0 PROGRAM SUMMARY

2.1 Preliminary System Design Approach

Initially, following the CMC processor a coherent QPSK demodulator was selected for implementation, in the satellite receiver. Optimal techniques for coherent demodulation of QPSK signals are well known. These techniques involve carrier tracking (Costas loop, quadruppling the QPSK signal followed by a phaselocked loop circuit, and remodulation technique)[2,4], which can be difficult when dealing with bursted signals as is the case when the QPSK signal is first passed through chirp transform processing (convolve-multiply-convolve, CMC) prior to demodulation. For each channel the QPSK modulated signal coming out of the CMC is within a narrow time span (in the order of 25 nanoseconds) repeated at the frame rate of the chirp generator, which is made to be the same as the QPSK signal symbol rate. Consequently, a fast carrier acquisition circuit is needed. The existing techniques are not suitable for these type of bursty signals. In light of this problem, initially differential phase shift keying (DPSK) was proposed, but not implemented due to an expected 2.3 dB penalty in performance degradation[4]. In this case symbol decisions are made based on two consecutive phases, with the assumption that the carrier phase reference remains constant during the decision interval. Recent advancement in DPSK technique, however, showed that its performance can be improved by maximum likelihood estimation based on more than two transmitted phases[3]. Through computer simulation it was shown that, for a QPSK signal, when symbol decisions are made based on 5 consecutive transmitted phases, the performance penalty is reduced to 1 dB, which is more attractive (see Figure 2-1). In reality, if a conventional coherent demodulation technique is used the performance degradation would be disastrous due to the carrier tracking problem. Therefore, the practical implementation of this technique, known as multiple symbol differential detection (MSDD)[3], is recommendable. In this Phase II effort, however, a coherent QPSK demodulation technique was considered.

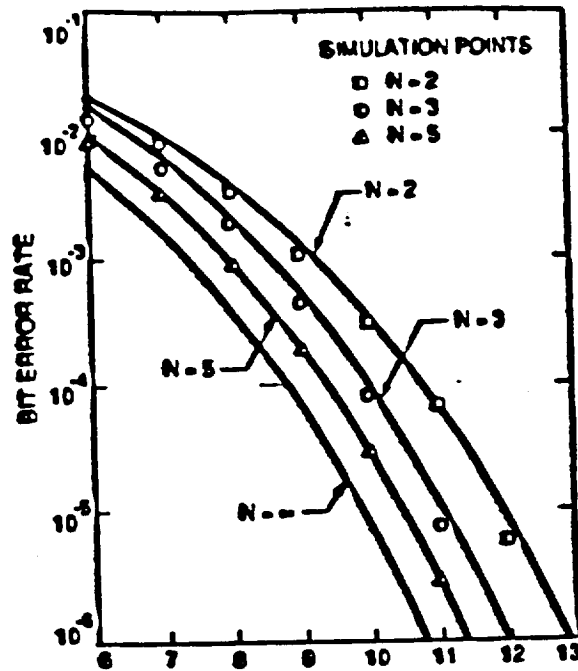


Figure 2-1:- Computer Simulation Result of BER Probability versus E_b/N_0 for Multiple Differential Detection of QPSK Signals.

Although MSDD was recommended for QPSK signal demodulation, after thorough consideration it is concluded that despite its advantages, this technique is difficult to implement because it necessitates the incorporation of several long delay lines (one symbol period equal approximately 30 microseconds) accurate to within 5 nanoseconds, while each channel only occupies a 25 nanoseconds interval. Such a delay line would normally be realized by acoustic wave devices, however, the required accuracy is extremely difficult to achieve. Consequently a different approach is considered, that is one utilizing a math-processor that computes the carrier phase reference in real time. It must be noted that as in the case of conventional coherent demodulation, a phase ambiguity exists that must be resolved utilizing differential encoding technique.

The mathematical representation of the received signal is as follows[2]:

$$s(t) = a_i \cos \omega t + b_i \sin \omega t \quad -T/2 < t < T/2 \quad (2.1)$$

The sine and cosine functions represent in-phase and quadrature-phase components of the QPSK signal. The received signal is split into two paths, where each is multiplied by a locally generated carrier signal having precisely the same frequency as the incoming signal

as shown in Figure 2-2. It is clear that its phase is arbitrary relative to the received signal phase. Without loss of generality this phase is represented by theta. The local oscillator signal is denoted by:

$$\sin(\omega t + \theta) \quad (2.2)$$

The in-phase component is labeled I, and the quadrature-phase component Q. The multiplication process generates 2ω frequency components that are suppressed by a lowpass filter. By utilizing trigonometric identities the resulting products are as follows:

$$\text{I-component: } a_i \sin(\omega t + \theta) \cos \omega t + b_i \sin(\omega t + \theta) \sin \omega t \quad (2.3)$$

$$1/2 a_i \sin \theta + 1/2 b_i \cos \theta \quad (2.4)$$

The shifted (90 degrees) version of this is:

$$I_{90} = 1/2 a_i \cos \theta - 1/2 b_i \sin \theta \quad (2.5)$$

$$\text{Q-component: } a_i \sin(\omega t + \theta) \sin \omega t + b_i \sin(\omega t + \theta) \cos \omega t \quad (2.6)$$

$$1/2 a_i \cos \theta + 1/2 b_i \sin \theta \quad (2.7)$$

The shifted (90 degrees) version of this is:

$$Q_{90} = -1/2 a_i \sin \theta + 1/2 b_i \cos \theta \quad (2.8)$$

Define X_{ic} , X_{is} , Y_{ic} , and Y_{is} as follows:

$$X_{ic} = I_{90} + Q = a_i \cos \theta$$

$$X_{is} = I - Q_{90} = a_i \sin \theta$$

$$Y_{ic} = I + Q_{90} = b_i \cos \theta$$

$$Y_{is} = -I_{90} + Q = b_i \sin \theta$$

Subsequently, the following quantities are derived:

$$\text{Q-component: } \|X\| = \sqrt{(X_{ic}^2 + X_{is}^2)} = \|a_i\| \quad (2.9)$$

($\|$ denotes absolute value)

If X_{ic} is not equal to zero, then $\theta = \tan^{-1}(X_{is}/X_{ic})$

and $X = \|a_i\| e^{j\theta}$, in this case chose $0 < \theta < 180^\circ$, and $a_i = X_{is}/\sin \theta$.

If X_{ic} is equal to zero, then $\cos \theta = 0$ and $\theta = (2n+1) \times 90^\circ$, chose $\theta = 90^\circ$ then

$$a_i = X_{is}$$

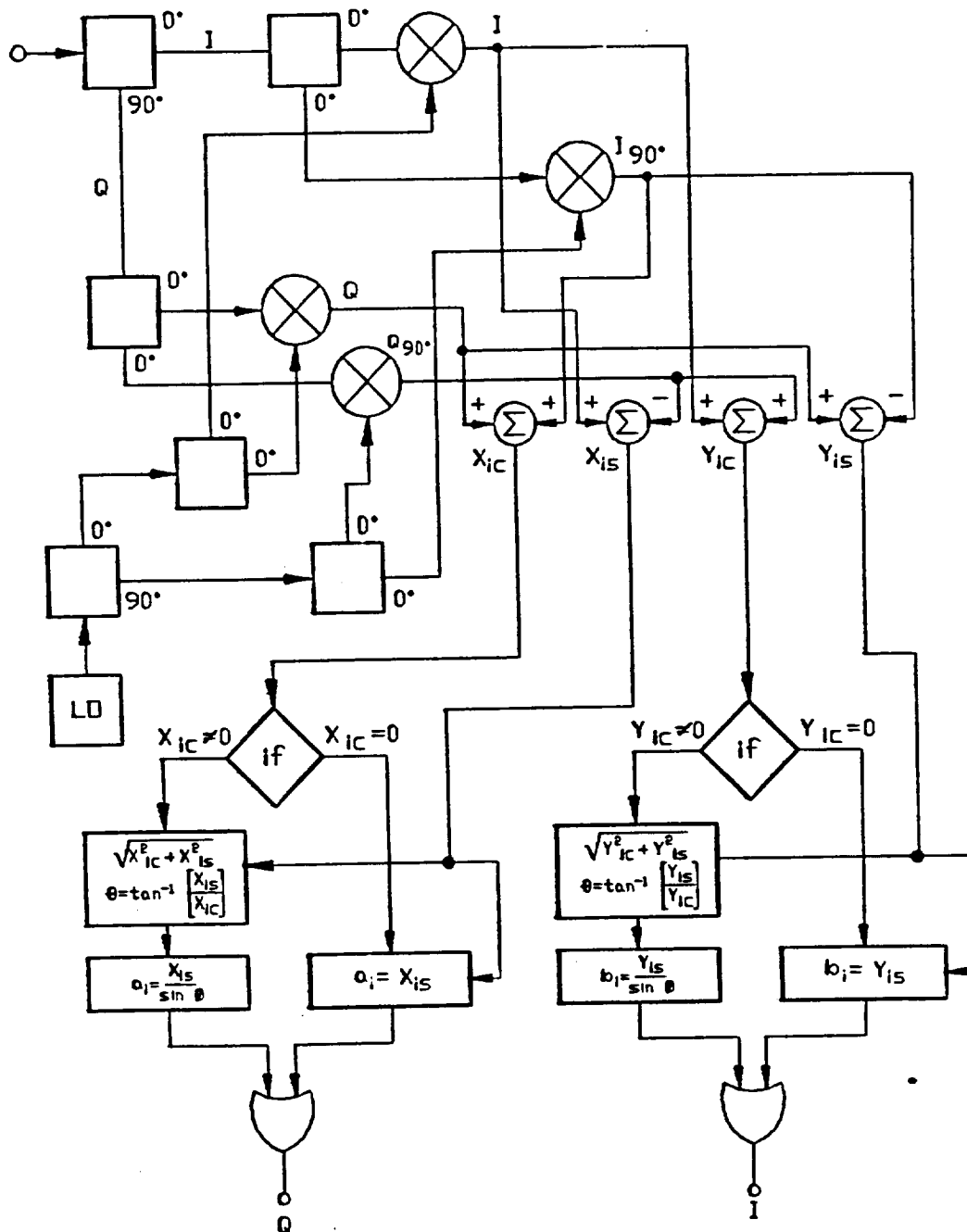


Figure 2-2:- Model for Coherent Demodulation of QPSK Signals.

If $X_{is} = 0$, $\sin \theta = 0$ and $\theta = nx180^\circ$, choose $\theta = 0$, hence $a_i = X_{ic}$

I-component

$$\|Y\| = \sqrt{Y_{ic}^2 + Y_{is}^2} = \|b_i\|$$

If Y_{ic} is not equal to zero, $\theta = \tan^{-1}(Y_{is}/Y_{ic})$ and $Y = \|b_i\| e^{j\theta}$, in this case $0 < \theta < 180^\circ$, and $b_i = Y_{is}/\sin$.

If Y_{ic} is equal to zero, then $\cos \theta = 0$, and $\theta = 90^\circ$, hence $b_i = Y_{is}$.

If $Y_{is} = 0$, then $\sin \theta = 0$, and $\theta = nx180^\circ$, choose $\theta = 0$, and $b_i = Y_{ic}$.

The implementation concept of the above algorithm is shown in Figure 2-2. All the user channels are demodulated by a QPSK demodulator, and the mathematical process of obtaining the reference phase is done in parallel for each channel. Theoretically all channels can be processed by one super fast signal processor, however it is presently not economical. Parallel processing would allow a processing time of up to 15 microsecond for each symbol detection. The concept of the signal processor is shown in Figure 2-3. The measured parameters X_{ic} , X_{is} , Y_{ic} , and Y_{is} are quantized by a set of Flash A/D converters (ADC). The resulting quantities are stored in 4 pairs of 4x1K high speed memories. For each channel (within a 25 nanosecond slot) two samples are taken and stored by clocking the converters at twice the signal bandwidth (80 MHz). For a communication system comprising 512 users (channels), 1 Kbyte memory is sufficient. The I and Q data are taken out of the memories at 15 microsecond intervals and processed within the same period by moderate speed digital signal processors. Consequently, each channel will be equipped with a pair of signal processors (I & Q) as shown in Figure 2-3.

The effect of differential encoding to resolve reference carrier phase ambiguity is tested by assuming various possibilities of the received phase. In OQPSK (off-set QPSK) the transmitter sends the I-symbols (in-phase) and Q-symbols (quadrature-phase) off-set by one data bit.

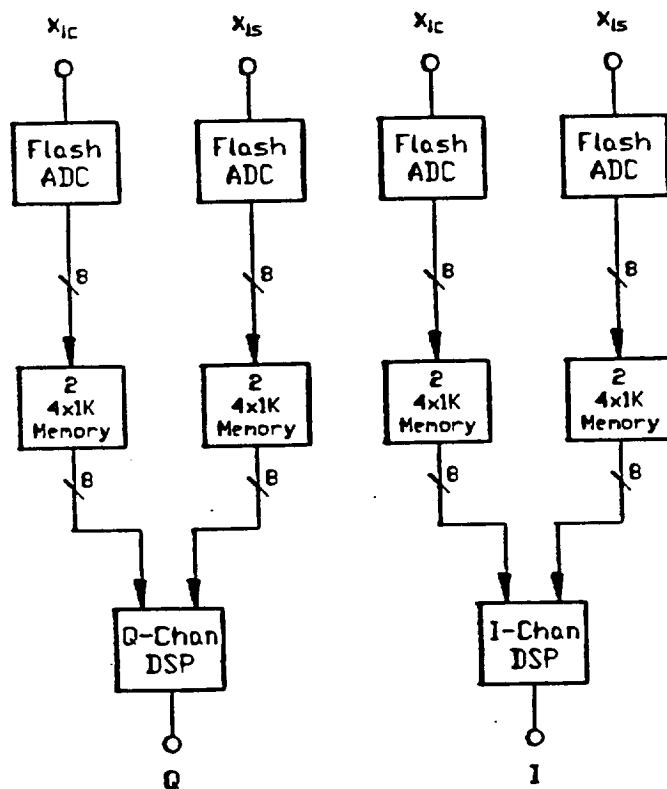


Figure 2-3:- Signal Processor for Coherent QPSK Demodulation

The outcome of the reference phase tracking circuit contains the following ambiguities:

Sent		Received		Comment
1.	I Q	I Q		No problem
2.	I Q	-I -Q		180° out
3.	I Q	Q (-Q) -I (I)		These two cases are basically the same
4.	I Q	Q I		
5.	I Q	-Q -I		

Case 2 through 5 are tested by sending a data pattern, split into I and Q streams, and differentially encoded prior to transmission. In the receiver an I and a Q stream are detected based on the recovered reference phase that contains the phase ambiguity.

Subsequently, the I and Q streams are differentially decoded and combined to reconstruct the transmitted data.

Definition of symbols:

I = Transmitted in-phase symbols

Q = Transmitted quadrature-phase symbols

Id = Differentially encoded I

Qd = Differentially encoded Q

Ir = Received I-stream

Qr = Received Q-stream

Ird = Differentially decoded Ir

Qrd = Differentially decoded Qr

Transmitter:

Data: 1 1 0 1 0 1 1 1 0 0 1 0 1 1

I: 1 0 0 1 0 1 1

Q: 1 1 1 1 0 0 1

Id: 1 0 0 0 1 1 0 1

Qd: 1 0 1 0 1 1 1 0

=====

Receiver:

Case 2 Ir = -Id, Qr = -Qd

Ir: 0 1 1 1 0 0 1 0

Qr: 0 1 0 1 0 0 0 1

Ird: 1 0 0 1 0 1 1

Qrd: 1 1 1 1 0 0 1

Data: 1 1 0 1 0 1 1 1 0 0 1 0 1 1

Case 3 $I_r = -Q_d, Q_r = I_d$

$I_r:$ 0 1 0 1 0 0 0 1

$Q_r:$ 1 0 0 0 1 1 0 1

$I_{rd}:$ 1 1 1 1 0 0 1

$Q_{rd}:$ 1 0 0 1 0 1 1

Data: 1 1 0 1 0 1 1 1 0 0 1 0 1 1

Case 4 $I_r = Q_d, Q_r = I_d$

$I_r:$ 1 0 1 0 1 1 1 0

$Q_r:$ 1 0 0 0 1 1 0 1

$I_{rd}:$ 1 1 1 1 0 0 1

$Q_{rd}:$ 1 0 0 1 0 1 1

Data: 1 1 0 1 0 1 1 1 0 0 1 0 1 1

Case 5 $I_r = -Q_d, Q_r = -I_d$

$I_r:$ 0 1 0 1 0 0 0 1

$Q_r:$ 0 1 1 1 0 0 1 0

$I_{rd}:$ 1 1 1 1 0 0 1

$Q_{rd}:$ 1 0 0 1 0 1 1

Data: 1 1 0 1 0 1 1 1 0 0 1 0 1 1

As can be seen in the above test that differential encoding is effective in resolving phase ambiguity. Differential encoding must be implemented on the I and Q streams respectively. Note that data randomization (for bit synchronization purpose), if required, has to be done prior to differential encoding.

2.2 Problems Encountered

For the CMC processor a HIRAC filter was designed, however, because of the high nonrecurring cost demanded by the vendor for fabrication and long delivery time, it was not implemented. For demonstration and proof of concept a RAC filter was implemented. This filter has a delay of 80 microseconds and 20 MHz bandwidth, resulting in a time-bandwidth

product of 1600.

The digital channel processor to recover the data from the I & Q demodulated signals, and circuits for data reconstruction were designed but not implemented, due to unexpected complex circuits required for sampling and processing the narrow pulses. These difficulties would have caused a delay and excessive cost to this Phase II program, beyond the budgeted time and money. Consequently, to obtain meaningful results within the specified time schedule a coherent BPSK demodulator was developed, built, and tested.

2.3 Final Implementation and Experiments

In light of the above mentioned problems a receiver was designed, developed, and tested, which comprises a CMC processor, a coherent BPSK demodulator, and a threshold detector for data reconstruction. To resolve phase ambiguities differential encoding and decoding are included. For testing purpose a BPSK modulator was designed as a test source. Subsequently, BER performance of this system was tested for various input signal E_b/N_0 , where E_b is the energy per bit and N_0 is the noise density. Gaussian noise is generated from a Hewlett Packard diode noise generator, followed by a bandpass filter and amplifier. Fixed attenuators are used to vary the E_b/N_0 . The following technical specifications for the receiver are established during test:

- | | |
|------------------------------|-----------------------------|
| a. Type of modulation: | BPSK |
| b. Data symbol rate: | 6.25 KBPS |
| c. Type of demodulation: | Coherent BPSK |
| d. CMC processor TB-product: | 1600 |
| e. Chirp filter bandwidth: | 20 MHz |
| f. Chirp filter slope: | .253 MHz/microsecond |
| g. Chirp filter type: | Reflective array compressor |
| h. Chirp repetition period: | 160 microseconds |

In this experiment, the data rate chosen was derived from the time delay and bandwidth of the RAC filter. As mentioned earlier the symbol period is made equal to the chirp

period. Since the RAC filter chirp slope is fixed (.253 MHz/microsecond) and the time delay of each filter is 80 microsecond, the chirp repetition rate required for a CMC processor must be 160 microseconds, hence the data rate is 6.25 KBPS. As a result of the prestructured technical parameters, the expected chirp transform pulsewidth is approximately 200 nanoseconds. At the output of the CMC processor, a chirp transform pulse appears every 160 microseconds (i.e. at the chirp repetition period). Its position in reference to the start of each chirp depends on the input frequency. Since the received symbol rate is equal to the chirp period, the polarity of the chirp transform pulses is directly related to each data symbol received. Therefore, the data can be recovered from the chirp transform pulses. To resolve phase ambiguities, differential encoding and decoding are implemented on the data respectively before transmission and after detection.

Coherent demodulation is obtained by injecting the BPSK demodulator with a signal that is in-phase with the received signal carrier.

3.0 WORK ACCOMPLISHED

3.1 Summary

The tasks, as defined in the statement of work, were *slightly* modified with the concurrent of the technical program office of NASA/Lewis. As a result of these, following tasks had been completed. The tasks were basically reflected in the system diagram shown in Figure 3-1.

- 1) The Design of Hyperbolic Inline Reflective Array Compressor Filter.
- 2) Development of Arbitrary Waveform Generator (Fabricated and Tested).
- 3) Demonstration of Chirp Transform Processor utilizing Amerasia's inhouse components.
- 4) Development of BPSK demodulator (Built and Tested).
- 5) Development, demonstration and documentation of system software to optimize the chirp waveform generated by the arbitrary waveform generator.

Utilizing the above listed sub-systems, system tests were conducted. In this test, Bit error rate as a function of input signal to noise ratio was measured and documented. To accomplish this test, a test source was built in the form of a BPSK modulator. The system test setup is shown in Figure 3-31.

3.2 Satellite Communications Receiver System Design

The detailed Satellite Communications Receiver System block diagram is shown in Figure 3-1. The RF portion normally associated with satellite receivers is not included in this design. It is assumed that the signal input to the receiver has been down-converted to the IF frequency centered at 100 MHz occupying a bandwidth of 32.768 MHz. This bandwidth covers 512 user frequencies each separated by 64 KHz. For proof of concept two user channels are included in the design. These channels operate in parallel and are physically identical. The main receiver, is designed to process the entire user population. However, each user channel must be equipped with its own channel processor, in this case two channel processors are provided. To resolve phase ambiguity in the demodulator the transmitted

data is assumed to have been differentially encoded.

The Advanced Communications Receiver consists of four units and individual Channel Processors. The input signal is composed of multiple user transmission frequencies operating independently from remotely located ground terminals. This signal is processed by the CMC Processor to transform each user frequency into a unique time slot. The CMC Processor is driven by a chirped local oscillator, which is derived from the SSB Modulator. The modulating signal to the SSB Modulator is a chirp waveform generated by the Chirp Waveform Generator (AMT-250). The QPSK Demodulator is the fourth major unit. The transformed QPSK signal is treated as a complex signal and coherently demodulated by means of a real time math-processor to obtain continuous phase tracking. The output of the demodulator is digitized and delivered to the Channel Processors. Each Channel Processor computes the carrier reference phase and makes symbol decisions. It also does the necessary differential decoding and I & Q data combining to reconstruct the transmitted data.

3.2.1 CMC Processor

The composite input signal to the CMC Processor is specified at a maximum level of -20 dBm. For 512 simultaneous channel users this means -47 dBm per channel in order not to overload the system. Comment: Since in practice the probability of all users operating at the same time is not 100 %, it would be possible to allow a higher level per user channel based on user statistics. However, this issue is beyond the scope of this project, therefore, will not be discussed any further.

The CMC Processor utilizes surface acoustic wave (SAW) devices that are inherently lossy (approximately 30 dB). To reduce the noise floor of the receiver a low noise amplifier is incorporated at the input. Linearity consideration of the CMC Processor is extremely important. In the front-end amplifier up to 512 different frequencies may be present at a given time. Therefore, any intermodulation products that falls within the receiver bandwidth would cause interference. The front-end amplifier is chosen to generate 3rd order intermodulation products that is less than 59 dB below the desired signal when fully loaded.

In the mixer this problem is exacerbated by the presence of several overlapping chirp signal frequencies. Therefore, a high level mixer is selected for this purpose. At the operating input level (-29 dBm) the third order intermodulation products are less than 110 dB below the signals. The choice of other amplifiers is based on the same linearity consideration. As a consequence of the input signal operating frequency band (83.6 MHz to 116.4 MHz) the chirped local oscillator frequency range is chosen within 167.2 MHz to 232.8 MHz and the upper sideband of the mixer is selected (283.6 MHz to 316.4 MHz). The resulting frequency plan guarantees adequate frequency separation among the inputs and output of the mixer, which simplifies the filtering requirement necessitated by nonideal isolation properties among the mixer ports.

The input SAW filter has a down-chirp response, with a slope of approximately 2.1 MHz/microsecond, and a time-bandwidth product of 512 which is equal to the number of resolvable frequencies. The chirped local oscillator has an up-chirp characteristic, with an opposite slope, and a time-bandwidth product of 2,048, i.e. 4 times the SAW filter time-bandwidth product. The output SAW filter has identical characteristics as the input filter, except its operating frequency is centered at 300 MHz. The SAW filters have a bandpass characteristic that approximates a rectangular shape, hence ideal for out-of-band spurious and interference rejection.

3.2.2 HIRAC Filter Design Study

The HIRAC development objective is to achieve a time-bandwidth-product of at least 3000. A conceptual layout is shown in Figure 3-2 in relation to a 3-inch LiNbO₃ wafer. Two transducers, one for launching and the other for receiving the sound waves are indicated by lines at the bottom of the wafer. Centrally located is the reflective array which causes the waves to be reflected from one transducer to the other. The incidence angle is 22.5° and corresponds to a direction of zero beam steering for the trigonal LiNbO₃ material. Also shown is the size of the enlarged Gerber layout border which is 19x25 inches before being reduced by 10X.

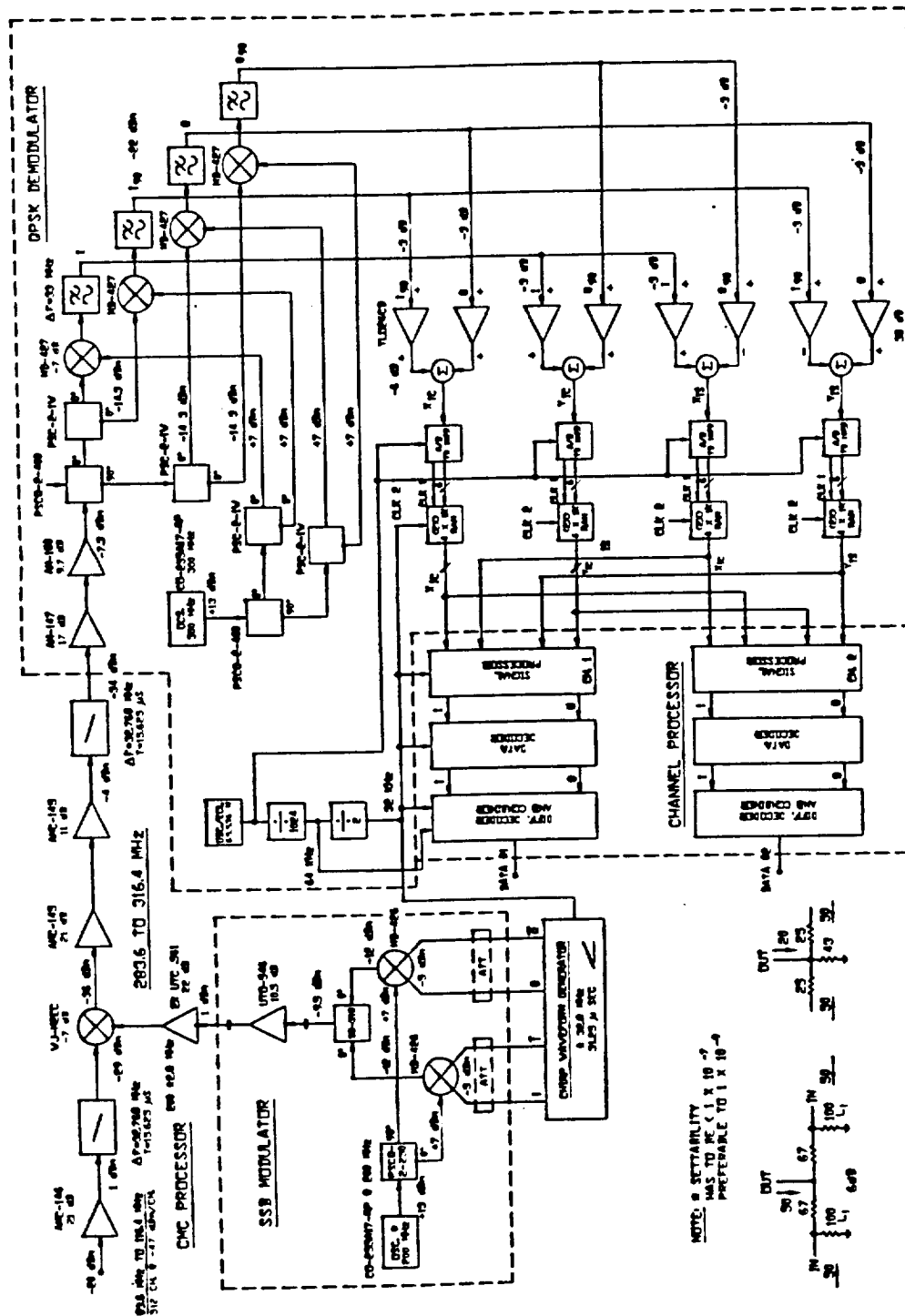


Figure 3-1:- Advanced Communication Receiver System Block Diagram

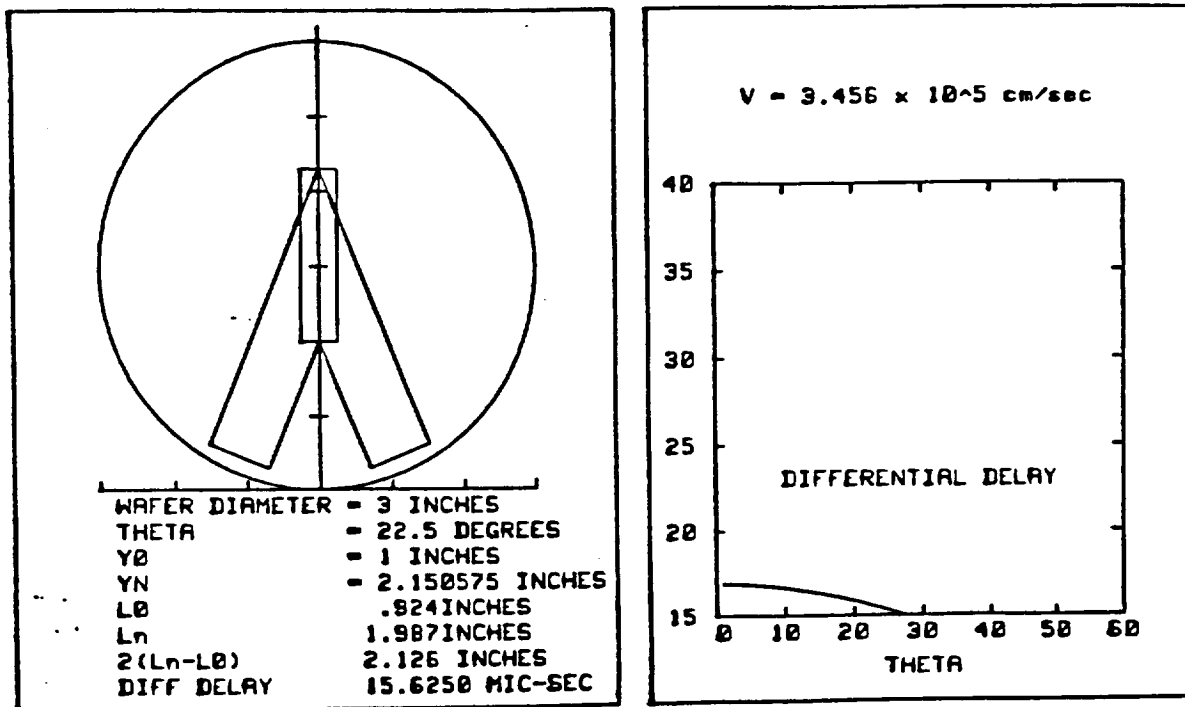


Figure 3-2:- Layout of HIRAC Filter

The complete design is shown in Figure 3-3. In this design four transducers are to be fabricated in such a manner as to generate an up-chirp and a down-chirp filter using the same reflective array.

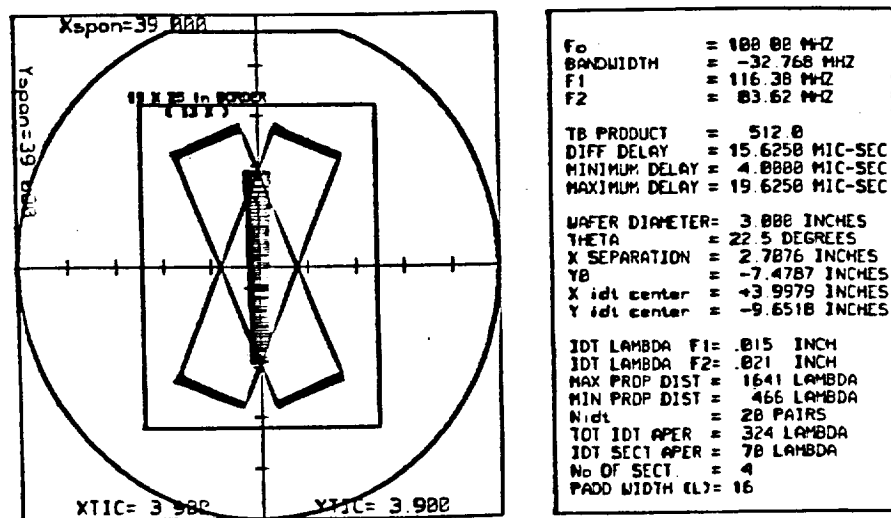


Figure 3-3:- Photomask Design Showing Both Up and Down Chirp.

The design of the transducers is complex, since most if not all of the important design parameters are determined by the transducer electrodes. In order to eliminate finger resistance effects and to achieve a hyperbolic frequency distribution, the transducers are split into channels as shown in Figure 3-4. Here the X dimension is greatly exaggerated compared with the Y dimension so that the fingers of the electrodes are shown clearly.

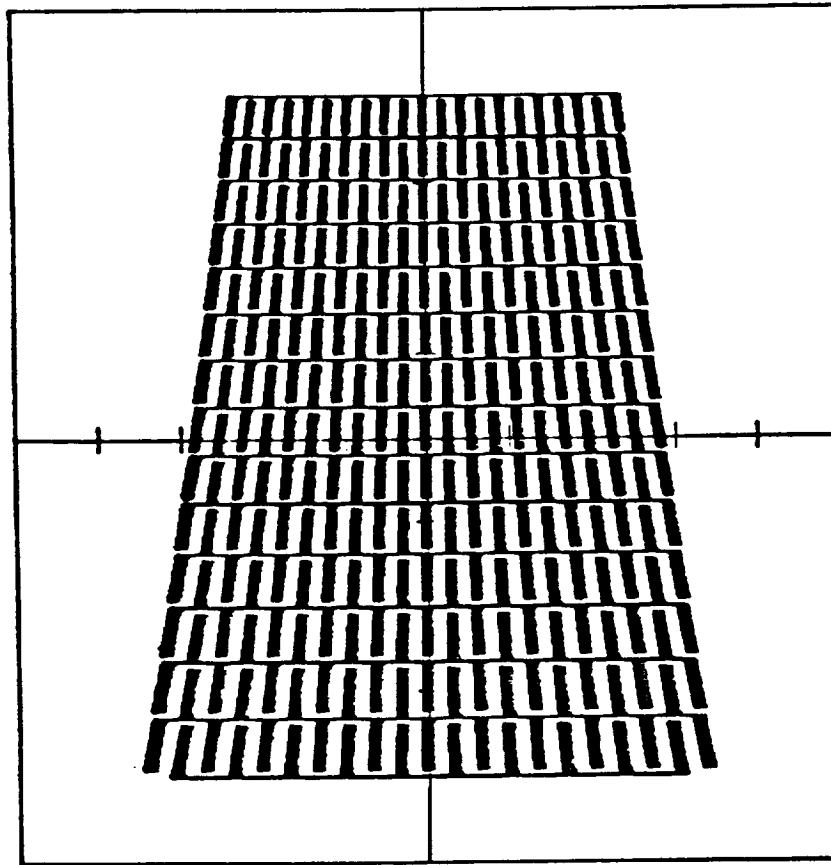


Figure 3-4:- Multichannel Transducer Layout, X-span = 0, Y-span = 0.2 inch.

Figure 3-5 shows a section of an actual transducer where the electrodes are drawn to scale and lying at the proper 22.5° angle so as to launch the waves at the proper reflective angle to the dispersive reflective array.

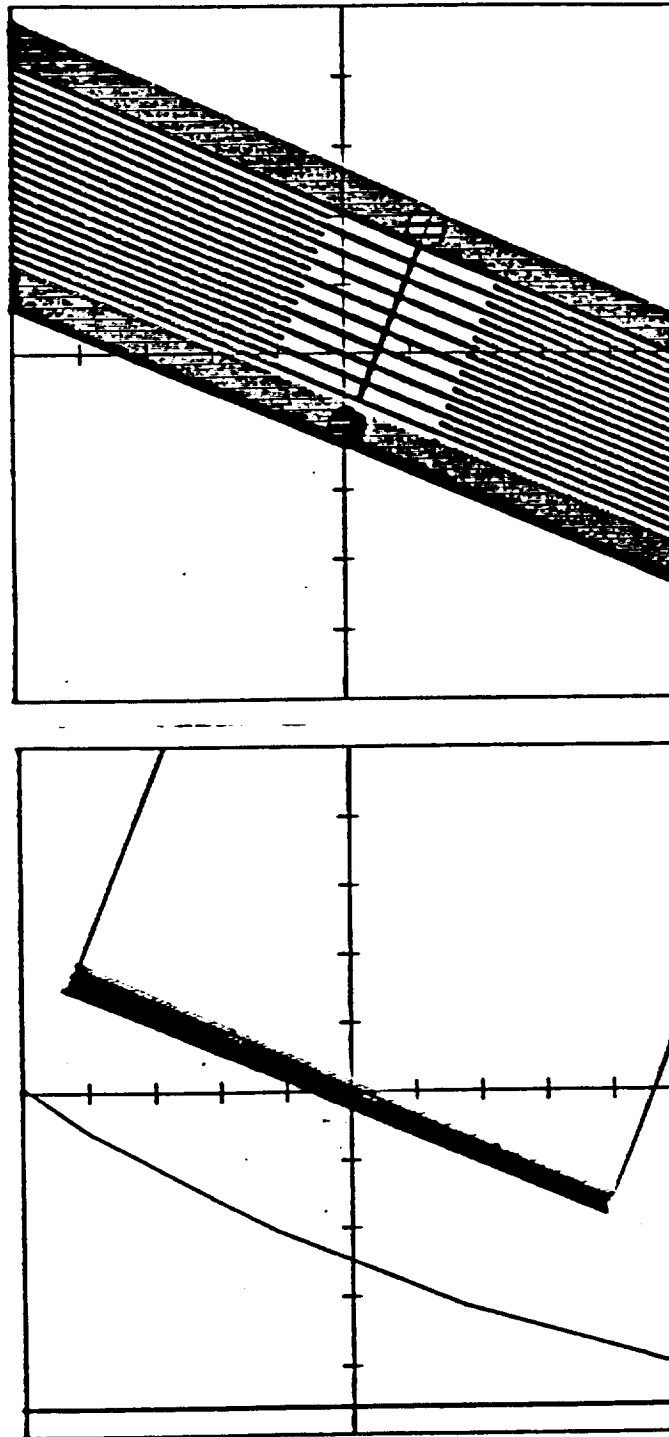


Figure 3.5:- A Section of An Actual Transducer

3.2.3 Chirp Waveform Generator

The Chirp Waveform Generator (AMT-250) is fully digitally implemented, combining high speed logic and signal processing techniques. A functional block diagram is shown in Figure 3-6 and a picture of the AMT-250 is shown in Figure 3-7. The design is a modification of an existing product developed by Amerasia Technology. The frame rate of this unit is 32 KHz, controlled by an external clock that is in synchronism with the sampling signal of the A/D converter located in the QPSK Demodulator. The time frequency slope of the chirp is programmable to match the SAW filter chirp slope. Temperature effect varying the SAW filter slope is compensated by software implementation in the Chirp Waveform Generator.

In Figure 3-6 only one of the two channels (I or Q) is shown. Each channel contains eight waveform memory chips labeled RAM A through RAM H. The RAM chips contain 8-bit waveform pixel data which is loaded into the RAMs from the microprocessor on the chirp interface board. A 12-bit counter selects the appropriate address of each RAM sequentially. The outputs from the RAMs are interleaved. Interleaving of RAMs A, B, through H is explicitly shown in the diagram. The interleaved RAM outputs are loaded in parallel into two 40-bit shift registers which are clocked into a high speed video digital to analog converter (DAC) which, subsequently, generates I and I^* data with 75-Ohm output impedance. The other channel generate Q and Q^* data in the same manner.

The chirp waveform generator board is a three layer board. The top view of the board layout is shown in Figure 3-8. In the center of the board four shift registers are shown. These registers provide parallel-in, and serial output at speeds up to 250 MBPS. Along the upper portion of the board are 16 RAM chips (U6-U21) which provide waveform memory. These RAMs are organized as 8Kx8 bits and a total memory of 64K for I and 64K for Q is possible. Just below and adjacent to the RAM arrays is a second row of 16 octal tri-state buffers used to put RAM data output onto the local buss. A local counter is used to derive RAM addresses (U1-3).

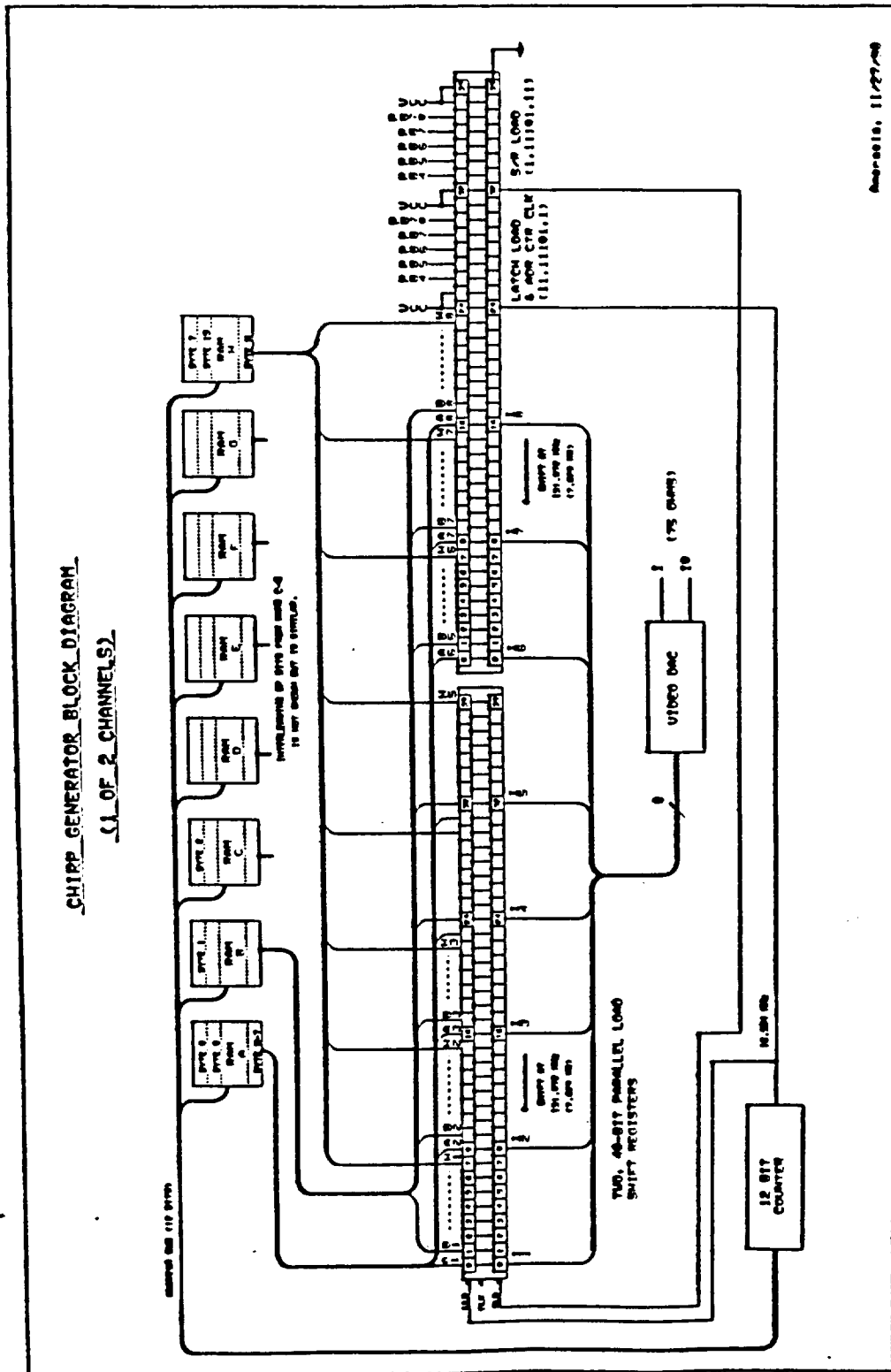


Figure 3-6:- Chirp Generator Block Diagram

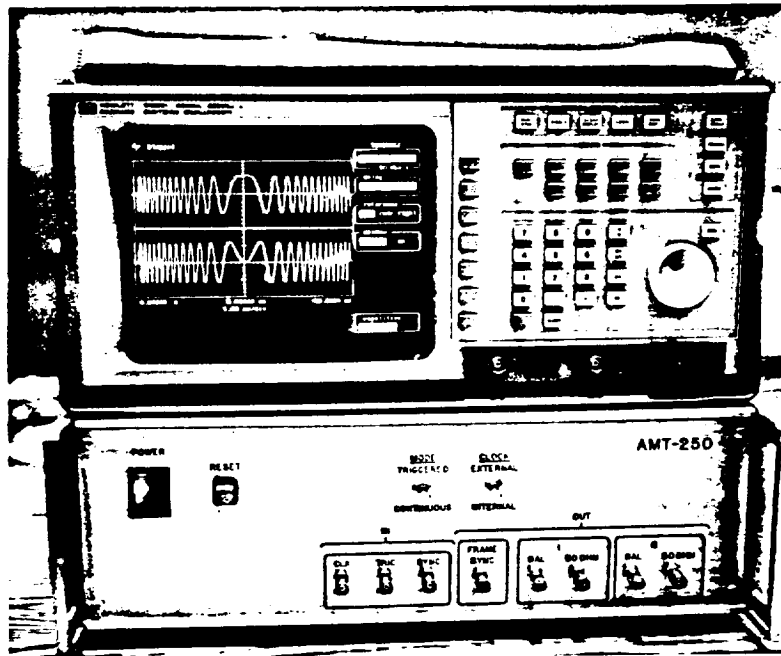


Figure 3-7:- Photograph of Arbitrary Waveform Generator, AMT-250.

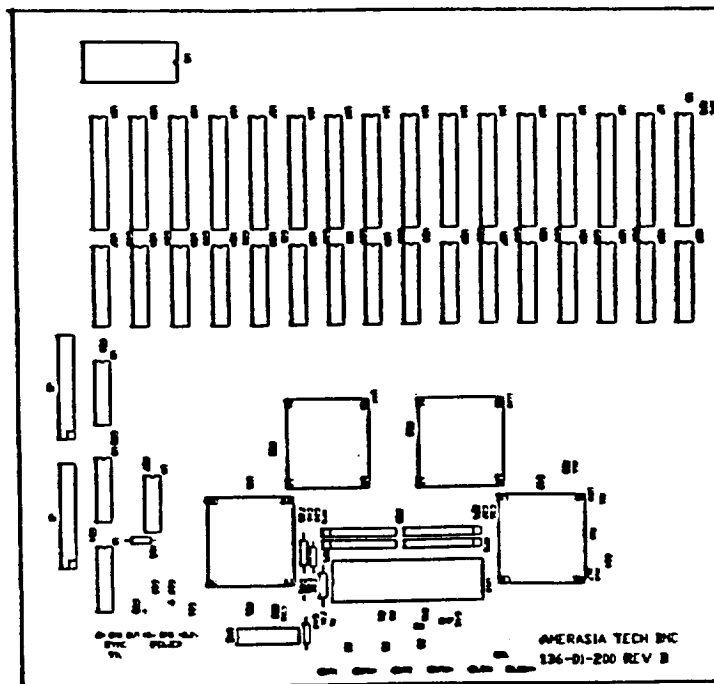
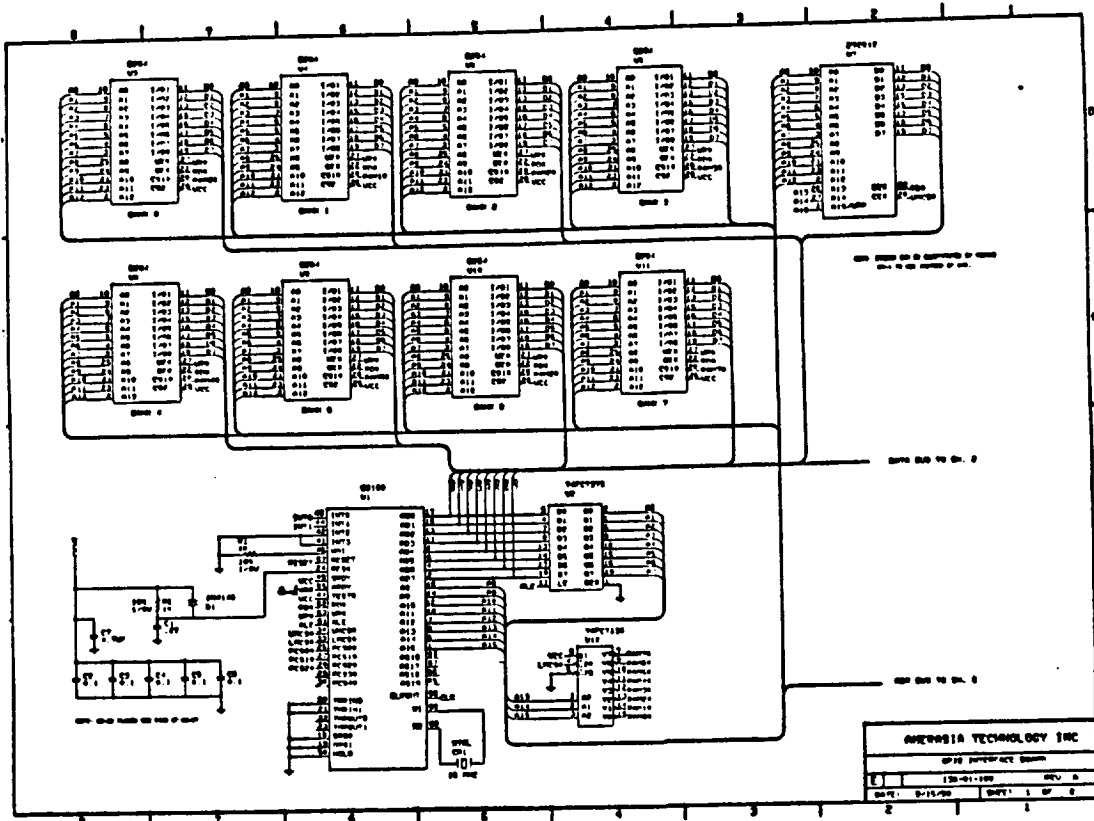


Figure 3-8:- Chirp Generator Board Layout

A computer interface board, containing a GPIB controller, is added to the control input of the arbitrary waveform generator, which allows for universal programmable waveform user interface. The circuit diagrams for GPIB interface are shown in Figures 3-9 and 3-10. Starting with Figure 3-9, U1 is the heart of the system microprocessor (Intel 80188). This microprocessor is a highly integrated member of the 8086 family. It was selected for its ability to generate I/O and memory selects. It also handles interrupt requests (priority) and contains an on-board clock. As a result the number of interface chips required to implement an imbedded microcontroller is minimized.

Program memory resides in the EPROM (U7, 27C512) which allows for 64K of program memory. Data memory is up to 64K and is contained in RAM chips U3-U11. Since the microprocessor utilizes multiplexed data and address technique, U2 provides the necessary latching of the low address bytes. Chip selects are generated by the decoder chip U12. The second part of the GPIB circuit, shown in Figure , contains the I/O peripherals which implements the GPIB, RS232, and chirp board interface functions. U13 is the GPIB interface chip which handles the necessary handshaking associated with the buss architecture. U18 and U19 are called buss interface chips that provide the correct routing and direction (transceivers) of the bi-directional GPIB signal lines. U14 implements the functions of the RS232 serial buss. U21 is a level shifter which translates the internal TTL levels to standard RS232 levels. Finally U15, technically a programmable peripheral interface chip, is used to download the chirp data to the chirp waveform generator board. Therefore, its output is compatible with the buss definition used in the chirp waveform generator board.

A second addition to the chirp waveform generator is an external synchronization circuit, called the SYNC/CLOCK and trigger circuit. The purpose of this circuit is to allow the chirp waveform repetition to synchronize with an external clock. In the advanced satellite receiver the chirp waveform has to be synchronized to the symbol timing of the received data.



The SYNC/CLOCK circuit is shown in Figure 3-11A and B. The clock to the address counters, on the chirp board, is gated by the doubly latched trigger signal from the trigger circuit shown in Figure 3-11B. This signal is asynchronous to the local clock of the chirp board. While awaiting a trigger signal, the address counters are held at the first memory address. After the trigger goes high, the next rising edge of the local clock causes the second subsequent data values to be output. The trigger signal must return to the low state prior to the end of the chirp waveform frame. Also the trigger pulsewidth must be greater than 100 nanoseconds for reliable operation.

3.2.4 SSB Modulator

In the SSB Modulator, shown in Figure 3-12, the baseband chirp waveform is translated to the desired operating frequency. The SSB Modulator has in-phase (I) and quadrature-phase (Q) inputs as required by complex waveforms. Each input is differentially configured to suppress any noise or undesired spurious components. Two doubly balanced mixers (M1 and M2) are used to modulate the I and Q signals separately. The I and Q local oscillator drives are derived from a common phase-locked oscillator (PLO) and split into sine and cosine related signals by a quadrature hybrid circuit (HY1). The mixer outputs are combined and amplified to drive the high level mixer in the CMC Processor.

After further system analysis it is found that to reduce the negative effect of various oscillator frequency instability, the frequency sources to generate the 200 MHz and 300 MHz signals (see the system diagram in Figure 3-1) must be derived from a single stable clock. The clock frequency selected is 20 MHz or 40 MHz. The circuit implementation for the latter case is shown in Figure 3-12, which depicts the SSB Modulator circuit. The frequency stability of the reference clock is better or equal to .1 PPM. Consequently, the receiver system frequency stability is only dependent on the stability of the reference clock. As shown in Figure 3-12, the 200 MHz source is derived from a 20 MHz reference signal which in turn is generated, by frequency division (U7), from a 40 MHz crystal oscillator

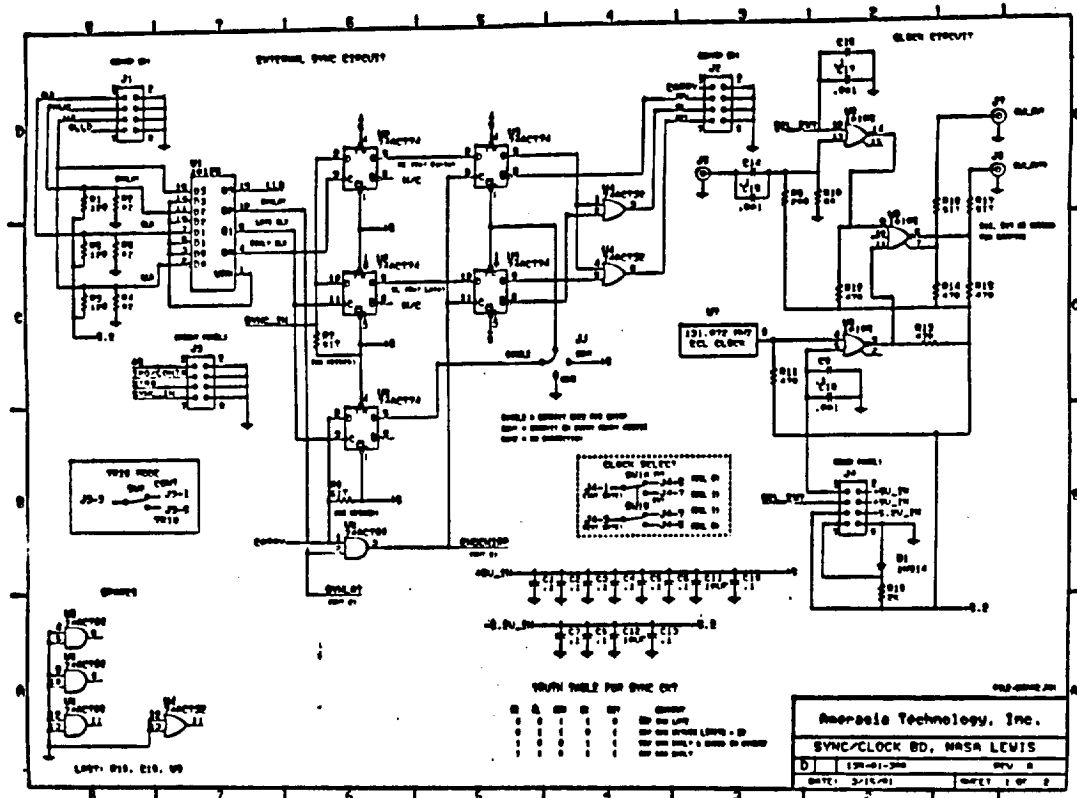


Figure 3-11A:- Sync/Clock Board

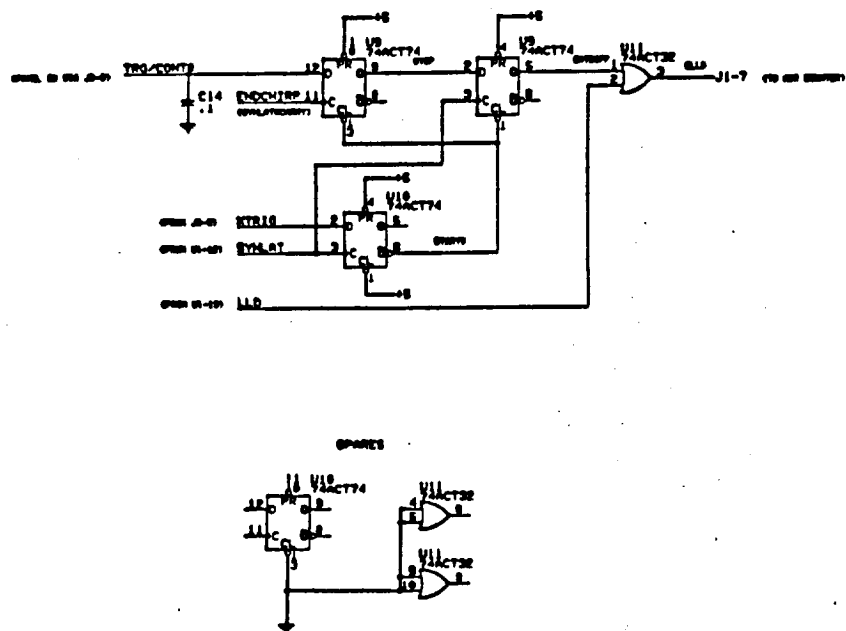


Figure 3-11B:- Continuation of Syn/Clock Board

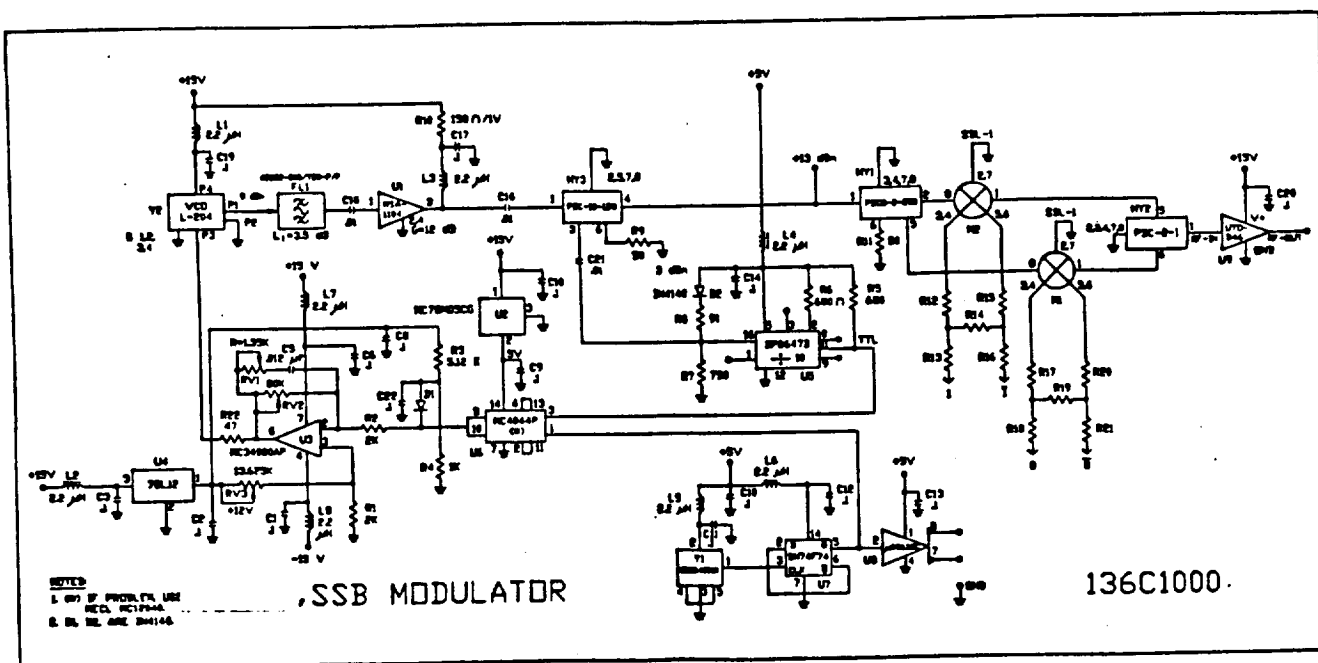


Figure 3-12:- Circuit Diagram of SSB Modulator

(Y1) in a phase locked loop (PLL). A 200 MHz signal is generated by the VCO (voltage controlled oscillator). The VCO output frequency is divided by 10 and compared with the reference signal in the phase comparator (U6). The output of the phase comparator controls the frequency of the VCO via U3. U3 and its associated circuitry establish the loop gain and frequency response of the PLL. The output of the PLL drives the in-phase and quadrature-phase balanced mixers (M1 and M2) of the SSB Modulator. The outputs of these mixers are combined by HY2, amplified, and routed to the CMC processor (see Figure 3-1). HY2 is an in-phase power combiner. The baseband inputs of mixers M1 and M2 are in a balanced configuration to cancel any DC offset created in the chirp waveform generator. Finally, the SSB Modulator will be implemented on a printed circuit board and packaged in an Aluminum enclosure for RF shielding.

The 300 MHz frequency source for the QPSK demodulator (see Figure 3-13) is generated in the same manner. In this case a 300 MHz VCO is locked to the 20 MHz reference signal.

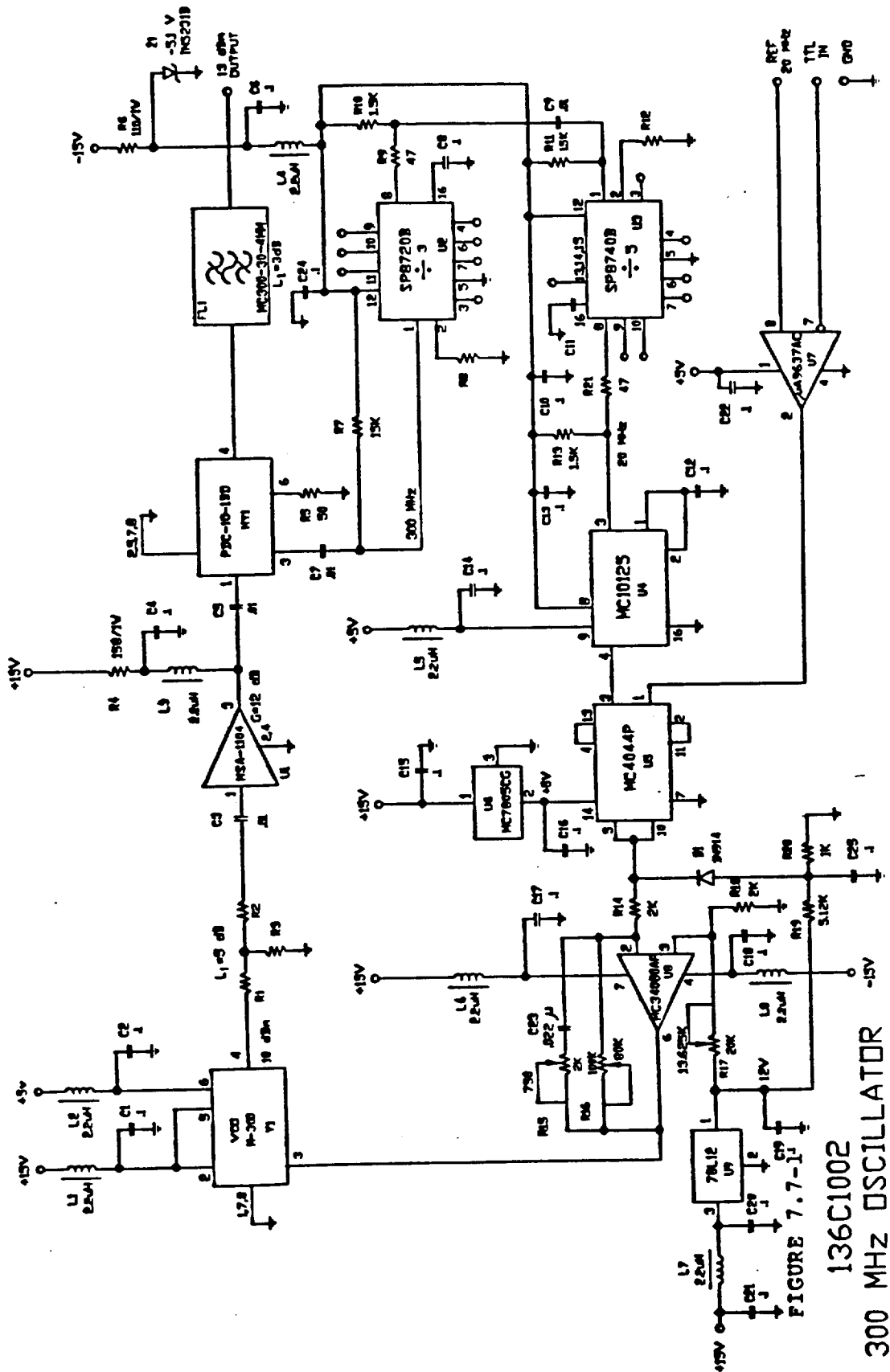


Figure 3-13:- 300 MHz Oscillator

The performance of the SSB Modulator is dependent on the performance of the available circuit components. Figure 3-14, shows a simplified block diagram of the modulator, where only components relevant to its performance are shown. These components are as follows:

- (1) Input Hybrid : Model PSCQ-2-250
- (2) Frequency Mixers: Model SBL-1
- (3) Output Power Combiner: PSC-2-1

Performance of each of the above components are limited by the following manufacturer's specifications:

- (1) Input Hybrid: Phase error is $.8^\circ$ Typ., 4° Max.
Amplitude error is $.6$ dB Typ.,
 1.5 dB, Max.
- (2) Frequency Mixer: RF to LO leakage,
typically -40 dB, -35 dB Max.
- (3) Power combiner: Phase error is $.5^\circ$ Typ.,
 4° Max.
Amplitude error is $.02$ dB
Typ., $.3$ dB Max.

In the analysis the input signal amplitude is normalized to one. Without loss of generality the input local oscillator (LO) signal to the modulator is represented by $\sin(\omega t)$, as shown in Figure 3-15. The I and Q inputs are distinguished by a 90° phase shift. These signals are modelled as $\sin(\omega_m t + 0)$ and $\cos(\omega_m t + \theta)$ respectively. Replacing the I signal by $\cos(\omega_m t + \theta)$ will not change the outcome of the analysis, because a 90° phase shift would result in a quadrature component represented by $-\sin(\omega_m t + \theta)$.

The output of the input Hybrid at point P (see Figure 3-14) is phasewise unaltered, while its amplitude is equal to $.707$. Therefore, at point C we have:

$$.707 \sin(\omega t) \sin(\omega_m t + \theta) \quad (3.1)$$

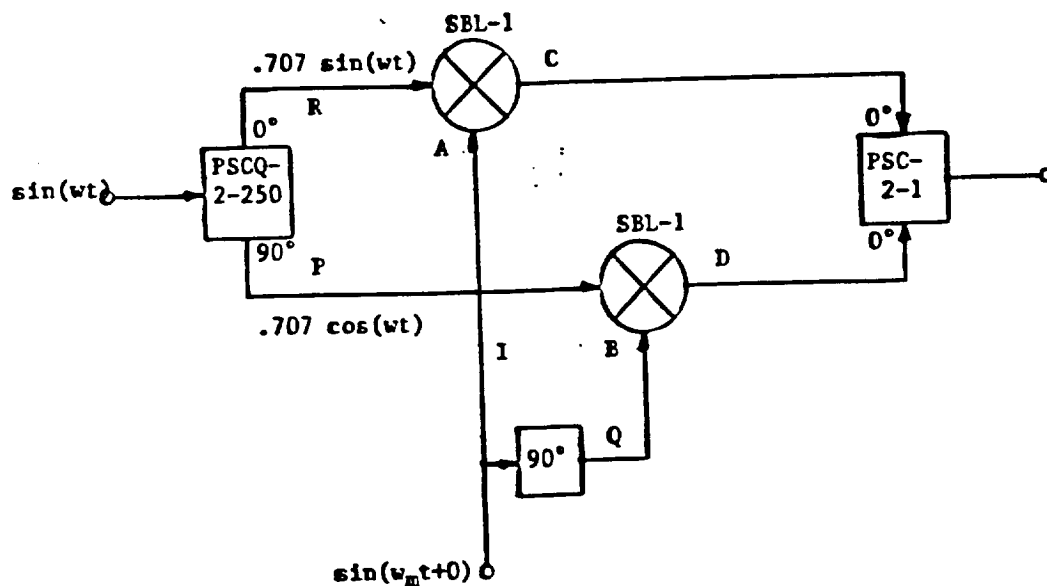


Figure 3-14:- Model of Idealized Modulator

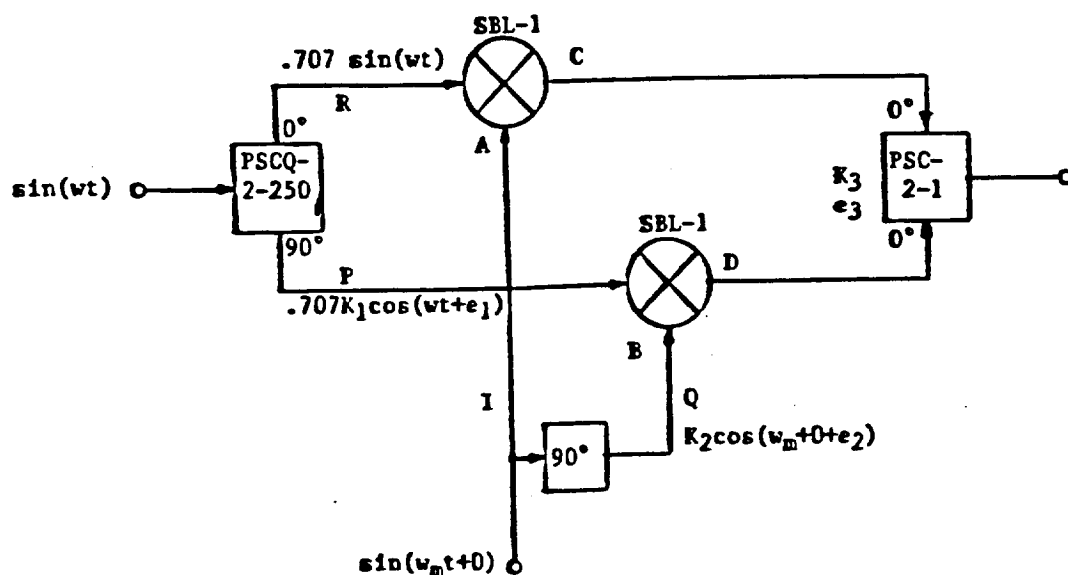


Figure 3-15:- Model of Nonideal Modulator.

The phase shifted version of the input signal is $\cos(\omega t)$, hence the signal at point D is:

$$.707 \cos(\omega t) \cos(\omega_m t + \theta) \quad (3.2)$$

The output combiner adds these two signals to produce:

$$.707 [\sin(\omega t) \sin(\omega_m t + \theta) + \cos(\omega t) \cos(\omega_m t + \theta)] \quad (3.3)$$

This is simply the lower sideband (LSB):

$$.707 \cos[(\omega - \omega_m)t - \theta] \quad (3.4)$$

If the I and Q inputs are reversed then:

At point C we get:

$$.707 \sin(\omega t) \cos(\omega_m t + \theta) \quad (3.5)$$

And at point D:

$$.707 \cos(\omega t) \sin(\omega_m t + \theta) \quad (3.6)$$

Combining (3.5) and (3.6) and applying a simple trigonometric identity we obtain the upper sideband (USB):

$$.707 \sin[(\omega + \omega_m)t + \theta] \quad (3.7)$$

As a result of the above analysis the desired sideband can be selected by making the appropriate I and Q connections as shown in the following table (Table - 1).

Table - 1

Input to		Output	
A	B	LSB	USB
I	Q	X	
Q	I		X

From the above analysis it can be concluded that under ideal conditions the modulator output:

(1) Does not contain any carrier components.

(2) Contains only one sideband.

Figure 3-15 shows the SSB Modulator model containing amplitude and phase error parameters introduced by nonideal components. K_1 , K_2 , and K_3 , are amplitude errors that can be equal or less than 1 but greater than 0. These parameters are associated with the input Hybrid, output power combiner, and input I and Q amplitude error, as shown in Figure 3-15. The phase errors are represented by e_1 , e_2 , and e_3 , which are associated with the Hybrid, power combiner, and input I/Q phase errors. The design implementation is such that K_2 and e_2 are adjustable to the point that their effect can be ignored. Subsequently, in the following analysis these two error parameters are neglected. The frequency mixer unbalance condition is treated as an RF to LO leakage and analyzed separately.

The analysis follows the same steps as described above. Hence, at point C we obtain:

$$\begin{aligned} &.707 \sin(\omega t) \sin(\omega_m t + \theta) = \\ &.707 \{ \cos[(\omega - \omega_m)t - \theta] - \cos[(\omega + \omega_m)t + \theta] \} \end{aligned} \quad (3.8)$$

and at point D:

$$\begin{aligned} &.707 K_1 \cos(\omega t + e_1) \cos(\omega_m t) = \\ &.707 K_1 \{ \cos[(\omega - \omega_m)t + e_1 - \theta] + \cos[(\omega + \omega_m)t + e_1 + \theta] \} \end{aligned} \quad (3.9)$$

Combining (3.8) and (3.9), while introducing the amplitude unbalance factor (K_3) and phase error e_3 , the output signal is obtained:

$$\begin{aligned} &.707 \{ \cos[(\omega - \omega_m)t - \theta] - \cos[(\omega + \omega_m)t + \theta] \} + \\ &.707 K_1 K_3 \{ \cos[(\omega - \omega_m)t + e_1 - \theta] + \cos[(\omega + \omega_m)t + e_1 + \theta] \} [\text{angle } e_3] \end{aligned}$$

The LSB and USB components are vectorially added. In this case the LSB component is the desired signal, while the USB component is undesired. Since e_1 and e_3 are phase shifts, for worst case calculations it is valid to combine the two phase errors ($e_1 + e_3$). The vector addition gives the following results:

The desired LSB component:

$$\begin{aligned} &.707 \cos[(\omega - \omega_m)t - \theta] \{1 + K_1 K_3 [\text{angle}(e_1 + e_3)]\} = \\ &.707 \cos[(\omega - \omega_m)t - \theta] \{1 + (K_1 K_3)^2 + 2K_1 K_3 \cos(e_1 + e_3)\} \end{aligned} \quad (3.10)$$

The undesired USB component:

$$\begin{aligned} &.707 \cos[(\omega + \omega_m)t + \theta] \{1 - K_1 K_3 [\text{angle}(e_1 + e_3)]\} = \\ &.707 \cos[(\omega + \omega_m)t + \theta] \{1 + (K_1 K_3)^2 - 2K_1 K_3 \cos(e_1 + e_3)\} \end{aligned} \quad (3.11)$$

The amplitude ratio between the undesired and desired (U/D) component is:

$$\frac{1 + (K_1 K_3)^2 - 2K_1 K_3 \cos(e_1 + e_3)}{1 + (K_1 K_3)^2 + 2K_1 K_3 \cos(e_1 + e_3)} \quad (3.12)$$

From the given components specification the error parameters were computed:

Typical performance,

$$K_1 = .9333 \text{ (-.6 dB)}$$

$$K_3 = .9977 \text{ (-.02 dB)}$$

$$e_1 + e_3 = 1.3^\circ$$

Substituting these values into equation (3.12) we obtain:

$$U/D = .0373$$

$$\text{In dBs, } U/D = -28.6 \text{ dB}$$

Worst case performance,

$$K_1 = .84 \text{ (-1.5 dB)}$$

$$K_3 = .966 \text{ (-.3 dB)}$$

$$e_1 + e_3 = 8^\circ$$

Hence,

$$U/D = .1253$$

$$\text{In dBs, } U/D = -18 \text{ dB}$$

Frequency mixer unbalance results in an unperfect RF to LO port isolation, which is typically 40 dB and in the worst case 35 dB. These quantities and the U/D values just calculated will be used in the CMC system performance analysis.

The performance of the SSB-Modulator is evaluated for undesired-to-desired signals (U/D) ratio, carrier frequency leakage (200 MHz), and frequency response. The test set-up is shown in Figure 3-16. For this purpose a test signal source has to be developed which will generate the I and Q signals to drive the SSB-Modulator inputs. The I and Q signal frequencies (f_I and f_Q) range from 0 to 35 MHz.

A test source was designed and built to test the performance of the SSB Modulator. The schematic diagram of the test source is shown in Figure 3-17. It consists of a Hybrid circuit to produce the 0° and 90° phase shifts. Frequency down conversion is necessary because it is difficult to find Hybrids that can operate from 0 to 35 MHz while simultaneously producing the desired phase shift with small amplitude and phase error. For this reason a Hybrid (PSCQ-2-400) which operates from 250 to 400 MHz is used. In the Test Source it is operated at a constant frequency (325 MHz), which acts as the local oscillator (LO) signal. This signal is down converted by mixers and an RF-signal ranging from 325 to 360 MHz to produce the desired I and Q signals (0 to 35 MHz). Identical lowpass filters at the outputs of the mixers suppress leakages from the LO and RF ports of the mixers. These filters are also designed to provide 50 to 100 Ohms impedance transformation, because the mixer output is 50 Ohms while the SSB-Modulator I and Q inputs are 100 Ohms. These outputs are connected to the SSB-Modulator via balanced twisted pair lines. The output of the Test Source is shown in Figures 3-18 and 3-19. Figure 3-18, shows the frequency spectrum which contains third harmonics of the desired signal, while Figure 8 shows the 90° phase shift between the I and Q signals. Since the Hybrid and Power divider used in the test circuit contain phase errors and amplitude unbalances (4° and .9 dB maximum) the output I and Q signals are not perfect. Consequently, it will make the SSB-Modulator appear to perform worse than its actual performance. As will be shown later the third harmonics of the I and Q signals show up at the output of the SSB-Modulator as spurious signals (see Table-2).

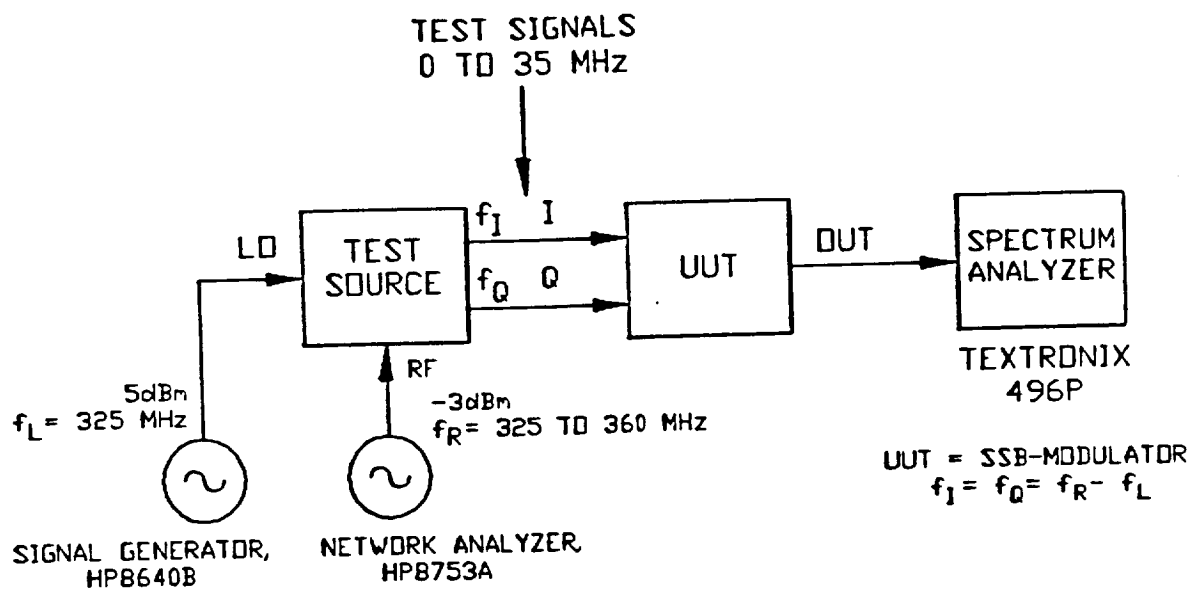


Figure 3-16:- Test Setup for SSB Modulator

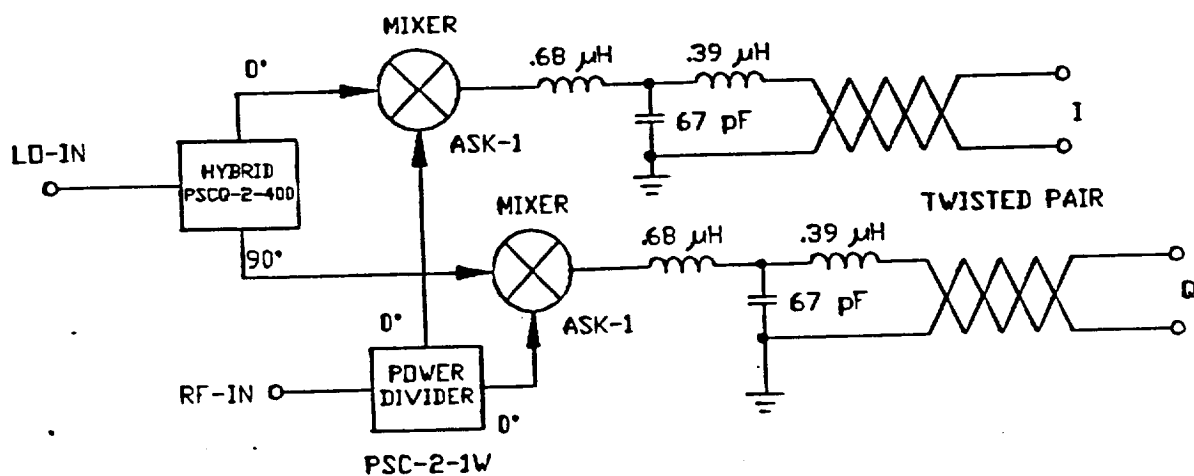


Figure 3-17:- Test Source Schematic Diagram

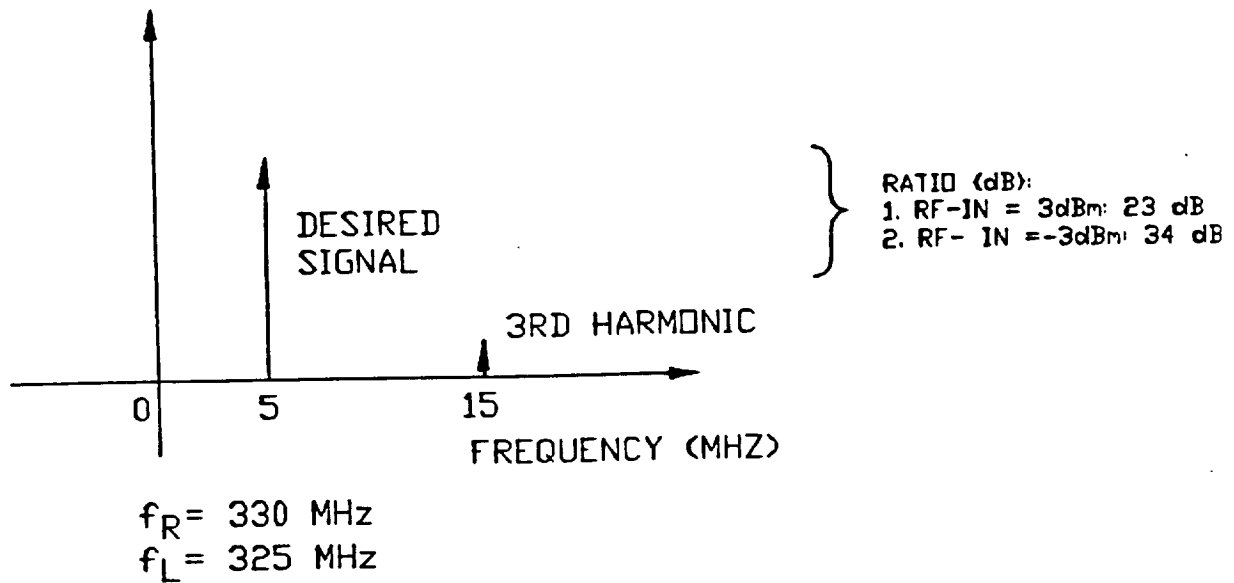


Figure 3-18:- Typical Frequency Spectrum of I Or Q Output of the Test Source

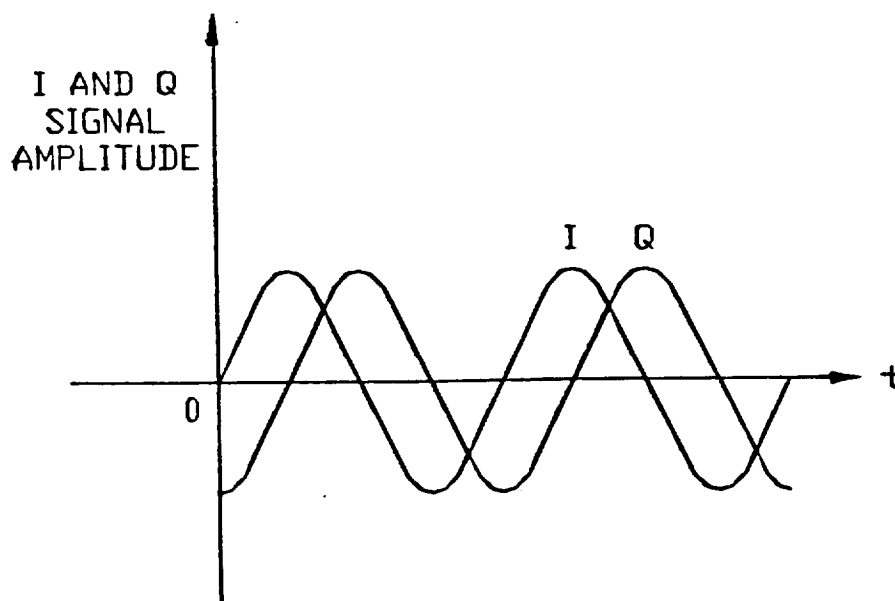


Figure 3-19:- I and Q Signal: From the Test Source

Table-2

f_R (MHz)	f_I or f_Q (MHz)	LSB (dBm)	U/D (dB)	Spurious* due to test signal	Comment
=====					
327.5	2.5	-15	-26	-39	
330	5	-15	-26	-39	
332.5	7.5	-15	-26	-40	
335	10	-15	-26	-40	
337.5	12.5	-15	-26	-41	
340	15	-15	-25	-42	
342.5	17.5	-15	-24	-50	
345	20	-15.5	-24	-47	USB/LSB
347.5	22.5	-16	-24	-48	USB/LSB
350	25	-16	-25	-50	USB/LSB
352.5	27.5	-16.5	-26	-50	USB/LSB
355	30	-17	-28	-50	USB/LSB
357.5	32.5	-17	-24	-50	
360	35	-17	-26	-50	
=====					

(*): Spurious signal related to $f_c \pm 3(f_R - f_L)$

Previous analysis showed that the expected U/D ratio of the SSB-Modulator, due to component phase errors and amplitude unbalance, is in the worst case -18 dB. The carrier frequency (200 MHz) leak of the mixers, in the SSB-Modulator, is maximum 35 dB below their LO level, which is 10 dBm. Consequently, taking into account the gain (12 dB) of its output amplifier the maximum expected carrier leak at the output of the SSB-Modulator is -13 dBm. The measured carrier leak output is -25 dBm, better than expected. As can be

seen from the test results in Table-2 and in Figure 3-20, the U/D (in this case Upper Sideband - to - Lower Sideband ratio) is -24 dB, that is, better than the expected worst case. In addition, the test signal is not perfect as mentioned earlier. Figure 3-20, also shows the amplitude-frequency response (LSB) of the SSB-Modulator, which is flat to 17.5 MHz and slightly rolls-off from 20 to 35 MHz. The spurious signals, $f_c \pm 3(f_R - f_L)$, is contributed by the third harmonic components of the test signal, thus not related to the performance of the SSB-Modulator.

3.2.5 QPSK Demodulator

The signal input to the QPSK Demodulator is amplified to a convenient level as shown in Figure 3-21. Each user channel data is confined in a 30.5 nsec time slot repeated every 31.25 microseconds hence the signal bandwidth at this point is 32 MHz. Adjacent time slots belong to other user channels repeated at the same rate. Since the signal is complex, its in-phase and quadrature-phase components are demodulated separately and subsequently combined. This is accomplished by generating the I, Q, and their shifted versions, i.e. I_{90} and Q_{90} . Four doubly balanced mixers are used for this purpose. Each mixer is driven by a sine and cosine related signal derived from a common 300 MHz oscillator via quadrature hybrid circuits, as shown in Figure 3-21. The outputs of the mixers are filtered, to remove harmonic frequency components, and combined in pairs as defined in Figure 4.0 by resistive combiners. Resistive combiners are used to establish an operating bandwidth down to the DC level. The combined outputs are digitized by 6-bit flash A/D Converters (ADC), sampled at the Nyquist rate. The 6-bit ADCs provide 36 dB resolution. The sampling frequency is synchronous with the Chirp Waveform Generator frame rate in order to guarantee optimum point sampling. For each user channel two samples per frame are taken to make a total of 1,024 samples per frame. These samples are stored in 6 x 1K RAMs (high speed buffers), each of which is composed of two 4 x 1K RAMs. The samples are kept within the RAMs for a period of 31.25 microseconds during which the reference phase must be computed and symbol decisions made for the I & Q data.

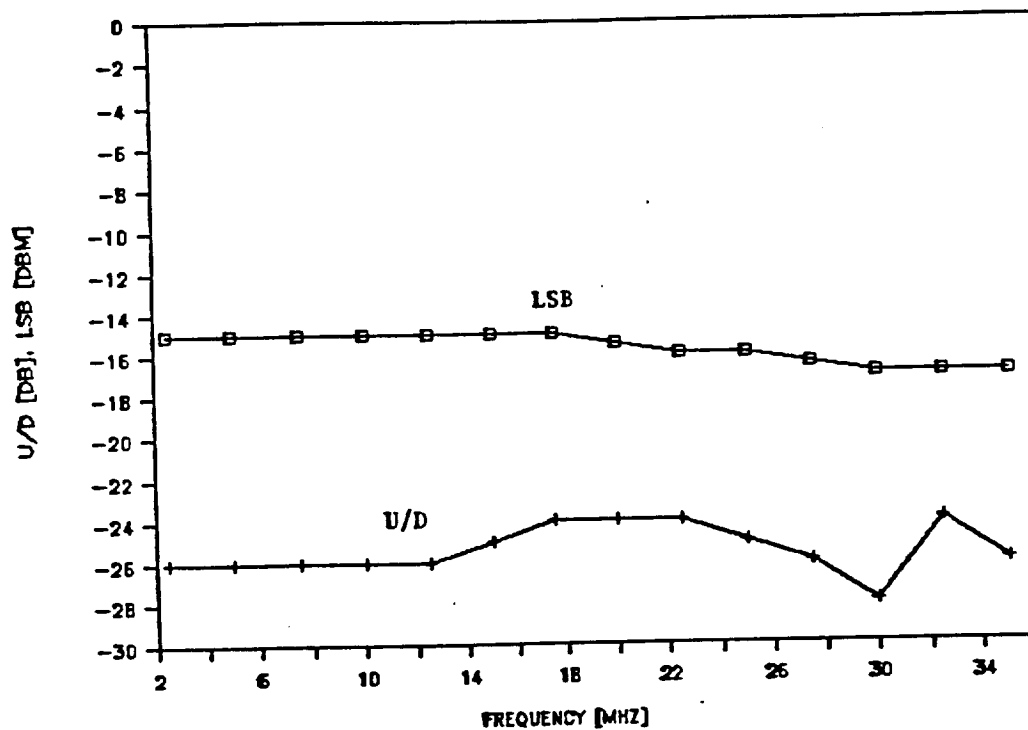


Figure 3-20:- Frequency Response of U/D, LSB

3.2.5.1 Implementation of the QPSK Demodulator

The QPSK Demodulator is driven by a 300 MHz Phase Locked Oscillator (PLO). The PLO is locked to a 20 MHz reference generated by a temperature compensated crystal oscillator (TCXO) located in the SSB Modulator. In doing so the frequency stability of the receiver is improved, which is important for carrier tracking.

The detailed circuit of the QPSK Demodulator is shown in Figure 3-21. The transformed output waveform from the CMC-Processor is composed of an RF carrier (300 MHz) embedded in a $\sin x/x$ envelope. The level of this signal is -34 dBm, which is amplified to -7.3 dBm by RF amplifiers U10 and U11. After amplification a small portion (-20 dB) of this signal is fed to a temperature compensation circuit, via the 20dB-coupler HY2. The larger part of the signal is sent to the demodulator, which comprises power hybrids, splitters, and balanced mixers. The demodulator detects the signal in each quadrant of the QPSK signal constellation. This is accomplished by splitting the input signal into I & Q (in-phase and quadrature-phase) components via hybrid HY3. The I component is further

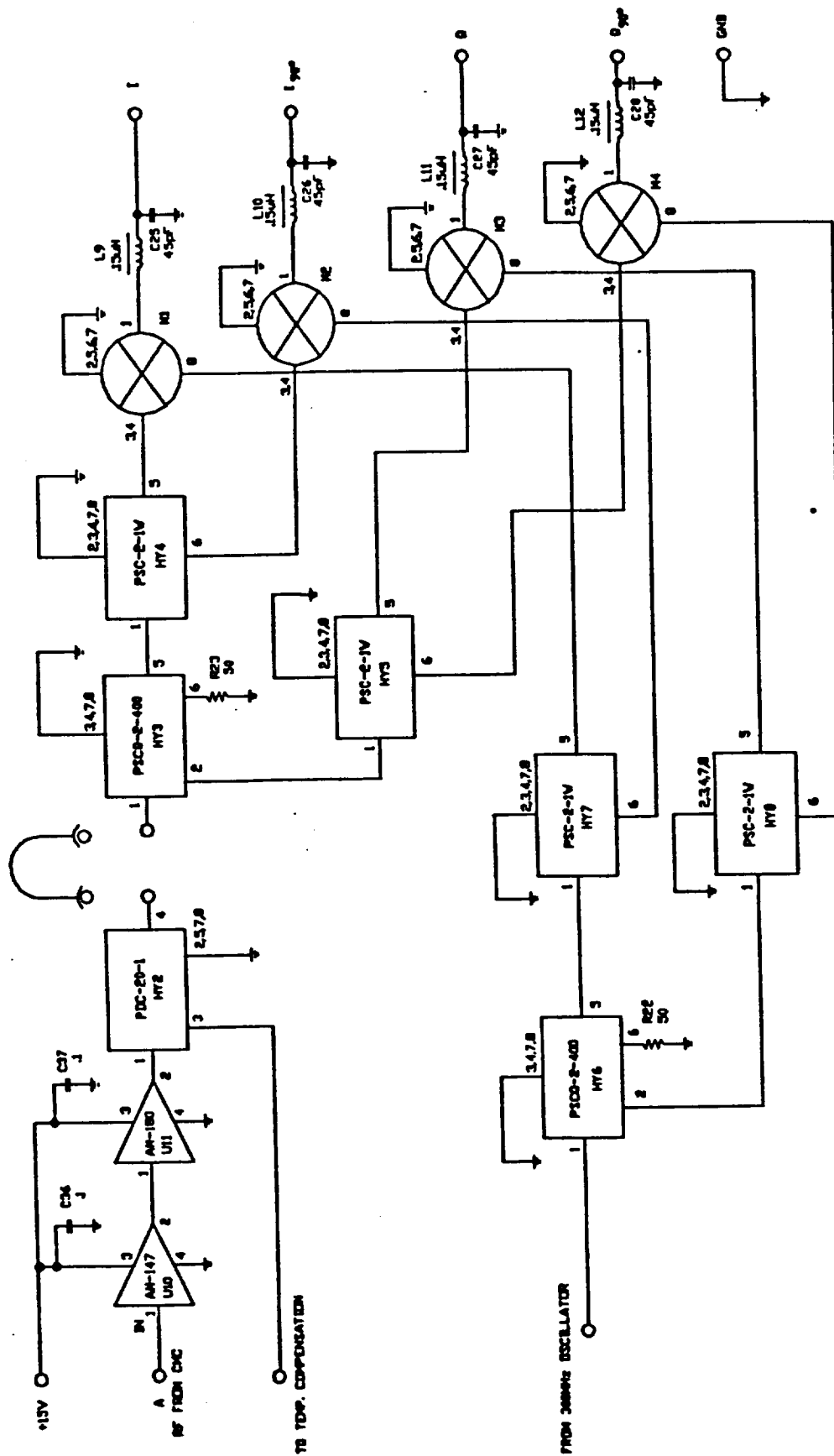


Figure 3-21:- QPSK Modulator

divided into two in-phase signals by HY4, which form the input to a pair of balanced mixers (M1 and M2). The Q component is treated the same way by HY5, and the resulting signals form the input to mixers M3 and M4. In the balanced mixers, the I and Q signals are multiplied by signals fed into their LO inputs. The output of these mixers are at the baseband level. Since the LO signals are also in in-phase and quadrature-phase forms, the mixers' outputs are also in in-phase and quadrature-phase forms. These LO signals are derived via hybrid HY6 and power splitters HY7 and HY8. By careful inspection of the demodulator circuit in Figure 7.6-1, it is easy to show that the outputs of mixers M1, M2, M3, and M4, that is I, I_{90} , Q, Q_{90} , are in quadrature relationship. The purpose of the lowpass filters at the output of each mixer is to suppress any RF frequency leak through the mixers. The filtered baseband outputs are processed by the following tracking and decision circuits.

3.2.5.2 300 MHz PLO

The detailed schematic diagram of the 300 MHz PLO is shown in Figure 3-13. The PLO is based on a conventional phase locked loop design. It is composed of a voltage controlled oscillator (VCO) Y1, frequency dividers U2 and U3, digital phase comparator U5, and DC-amplifier/filter U8. The 20 MHz reference signal is upgraded by a TTL line receiver U7, which feeds one of the input ports of phase comparator U5.

Initially, the VCO is tuned to approximately 300 MHz a portion of which, derived by directional coupler (10 dB) HY1, is fed into frequency dividers U2 and U3. These frequency dividers are ECL devices, which divides the input frequency by 3 and 5, respectively. The output frequency from the dividers, 20 MHz, is compared to the reference frequency by phase comparator U5. Prior to entering the phase comparator this signal is converted from ECL to TTL format. An error signal is generated by U5 is amplified and filtered by U8. The filter sets the loop response of the PLO. Subsequently, the DC signal from U8 corrects the frequency of the VCO until the error signal is reduced to zero. At this point the PLO is locked to the reference (20 MHz) signal, and its stability is controlled by the TCXO. The output (13 dBm) of the PLO is filtered by FL1, which is a bandpass filter

centered at 300 MHz.

3.2.6 Channel Processor

The Channel Processor receives fresh data every 31.25 microseconds and computes the carrier reference phase and makes symbol decisions within that period. The I and Q data are processed separately and the results are routed to the data decoder. The data decoder simply converts the symbols produced in the form of narrow pulses, by the signal processor, into its original form at the symbol rate (32 KHz). The recovered I and Q data are subsequently differentially decoded and combined in a parallel-to-serial combiner clocked at 64 KHz to form the final data output.

A block diagram of the digital channel processor is shown in Figure 3-22, consisting of four A/D converters (TDC1029). These converters operate at a sampling rate of 65.536 MHz and drive identical circuits for each channel. For demonstration purpose only two channels are implemented. The design of the channel processor is dictated by the QPSK signal timing architecture after demodulation. A timing diagram outlining this architecture is given in Figure 3-23. The first line of the diagram represents the chirp transform pulses after demodulation. Information from any channel appears in a time multiplexed order every $15.536 \mu\text{sec}$ (this corresponds to half the symbol period of QPSK data; the symbol rate is 32 KSPS for a bit rate of 64 KBPS). Because the symbol period is $31.25 \mu\text{sec}$ and the sampling rate is 65.536 MHz, while the chirp transform pulsewidth is approximately 30 nanosec, there are four samples of each QPSK symbol in any one channel. The second and third lines in the diagram show the two sample clocks, i.e. CLK-A and CLK-B, and their timing relationship to the chirp transform pulses. The fourth and subsequent lines show the clock, data and control waveforms on an expanded scale. Note the data latency of three clock cycles in the ADC. The following events can be seen from the timing diagram:

Sample 1-2 interval: 15.259 nanosec

Sample 2-3 interval: 15.610 μ sec

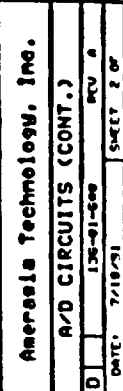
Sample 3-4 interval: 15.259 nanosec

Obviously the short time (15 nanosec) between samples 1 and 2 does not allow sufficient time to process the samples as each is received, however, the relatively long interval between samples 2 and 3 (15 μ sec) allows ample time for processing.

The delay from the start of the chirp transform pulse to the first sample is 15.259/2 nanosec, so that timing jitter must be substantially less than 7.6 nanosec to avoid sampling errors.

Based on the above technical considerations it is found necessary to store the samples prior to processing. A suitable realization is to utilize four 6-bit latches to store samples 1 and 2, followed by samples 3 and 4. These latches must be 100K ECL devices to reduce timing error due to propagation delay variations and finite risetime. As shown in Figures 3-24 and 3-25. Each sample of the chirp transform pulses Xic, Xis, Yic, and Yis, derived by the QPSK demodulator, is processed by an algorithm as described in paragraph 2.1, by using the two 6-bit samples to form a 12-bit address into a look-up table stored in a ROM. An additional advantage of this approach is the flexibility of modifications by simply programming a new ROM table. The intermediate results from the table look-up are clocked into a state machine whose transitions depend on the look-up results. After being clocked for each sample pair, the summer outputs a logic "1" unless at least three samples were logic "0". The I and Q data thus obtained are interleaved in the multiplexer and input to a differential decoder. The recovered data is taken from the decoder output. It must be noted that in this whole process data clock has been retrieved independently.

The Xic, Xis, Yic, and Yis inputs are each converted into 6-bit digital values in four identical circuits as shown in Figures 3-24 and 3-25. These four input signals derived from the QPSK demodulator are digitized in the 6-bit A/D converters U3, U4, U10, and U11, that are clocked at 65.536 MHz. The op-amp and emitter follower circuits provide temper-



-47-

ature stable upper and lower reference voltages to the A/Ds and set the input signals in the middle of the conversion range. The ECL digital outputs are bussed to the channel processors, one of which is shown in Figures 3-26 and 3-27.

Each 6-bit output is latched at times corresponding to samples 1 and 2 or 3 and 4 of the desired channel. Each channel uses eight, ECL latches U1 to U8 as shown in Figure 3-26. The 100K family of ECL logic is used because the subnanosecond propagation delays and rise/fall times are sufficiently small to maintain nanosecond timing accuracy. After the second and fourth samples there is approximately 15 μ sec to process the data. Conversion to TTL levels is done by the 100125 ICs, U9 to U16, to form 12-bit addresses into the algorithm look-up ROMs shown in Figure 3-27. For each sample the output of the algorithm is either a "1" or "0", and the digital summer sees a 2-bit input for each sample pair. The summer is a state machine whose transitions depend on the two inputs and their present state when clocked, and is implemented in programmable logic. The timing circuits provide two clocks for each symbol interval, causing the summer to output a "1" if at least three of the four samples were 1's. If two or less samples were 1's, a "0" is output.

After the fourth sample has been processed (near the end of a symbol period) the outputs of the two summers are multiplexed into the MUX/Decoder, which differentially decodes the data. These functions are also implemented in programmable logic arrays. Serial data is output along with a data sync pulse to facilitate transfer to the receiving device.

3.3 Revised System Design

As mentioned earlier due to schedule and funding constraint the a RAC filter was implemented for the CMC processor, and BPSK demodulation was implemented. However, the basic system architecture remains unchanged. In an earlier discussion it was established that the system design parameter is tailored to the RAC chirp filters' performance specifications. In this case the RAC filter has a 20 MHz bandwidth and a time delay of 80 μ sec, resulting in a chirp slope of .253 MHz per μ sec. Consequently, the chirp transform proces-

processor, of the convolve-multiply-convolve (CMC) type, has to be excited by a chirp waveform with a repetition period of twice^[1] the length of the chirp filter delay, i.e. 160 μ sec. Each data symbol of the incoming BPSK signal is made to coincide in time with each period of the chirp waveform. During this period the transformation process occurs. Since in a BPSK modulation system the symbol rate is equal to the bit rate, the data bit rate of this system implementation is 1/(160 μ sec) or 6.25 KBPS. To insure the chirp waveform and the incoming data to be in synchronism, data clock must be recovered. In this experiment it is assumed that data clock is available.

A block diagram of the CMC processor is shown in Figure 3-28. The input filter has an impulse response of a down chirp, implying that low frequency signals are delayed more than high frequency signals. The center frequency of this filter is 70 MHz. The incoming signal is multiplied with a chirp waveform that has an opposite slope in the mixer (ZFM-1W). The chirp waveform is called the expander, which has to have a bandwidth and period that is twice that of the chirp filter^[1]. The baseband chirp waveform is generated by the AMT-250, which is translated to a center frequency of 200 MHz by the SSB modulator. The output center frequency of the signal from the mixer is centered at 270 MHz, as shown. Since the output chirp filter center frequency is also 70 MHz a second mixer is used to downconvert the expanded input signal to within the passband of the output chirp filter. The output chirp filter has an identical impulse response as the input filter. Both filters have a bandwidth of 20 MHz. The chirp filters are the RAC type and have a delay of 80 μ sec. The performance of the CMC processor has been evaluated and the results are attached in the appendix.

3.3.1 BPSK Test Modulator and Data Encoder

A BPSK modulator and data encoder were designed, built, and tested to be used for testing the performance of the satellite receiver. The BPSK modulator/encoder is shown in Figure 3-29A. The design is tailored to interface with BER test set model HP 4925B, which has a RS-232 interface. Since the RS-232 interface chip contains TTL-RS232 level conver-

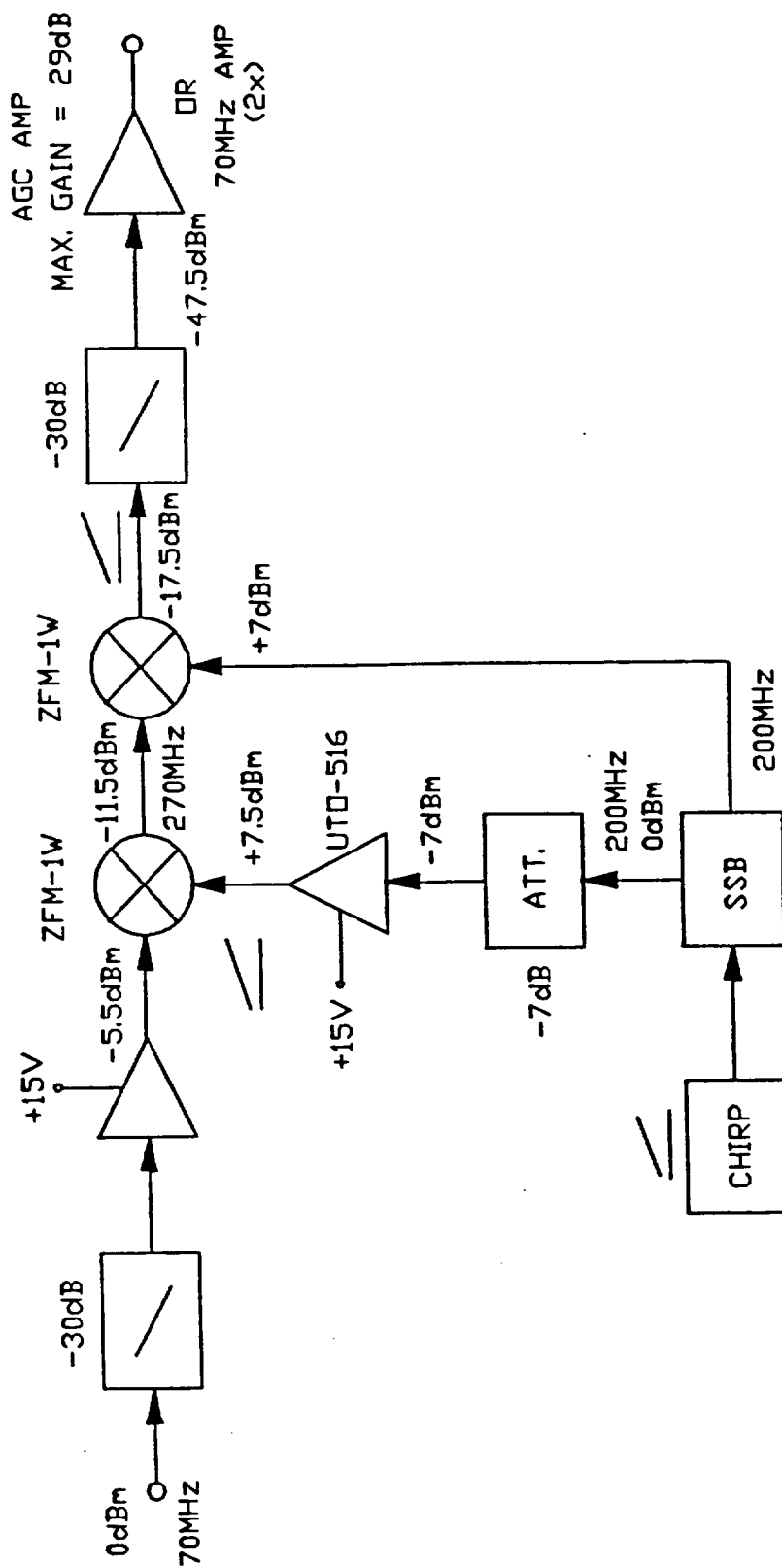


Figure 3-28:- Block Diagram of CMC Processor

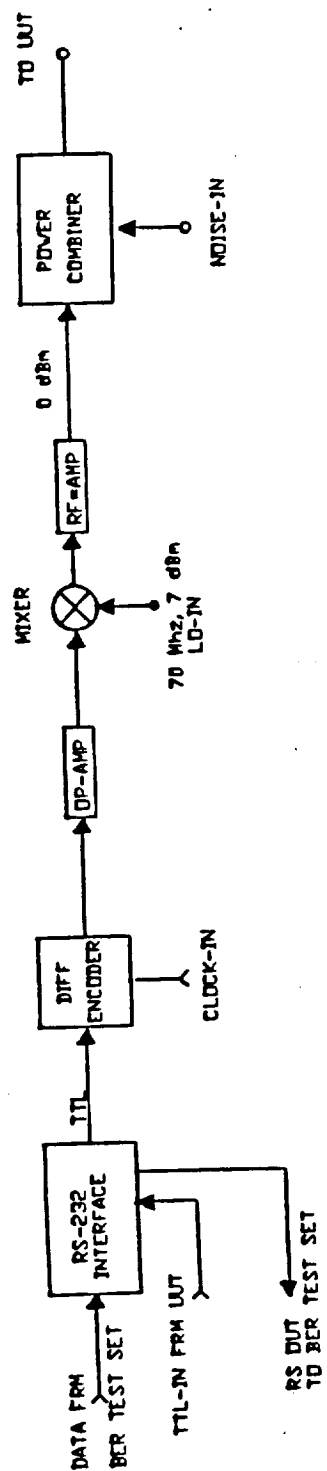
sion circuits in both directions, the recovered data from the receiver, which is in TTL format, is also input to this chip for conversion to RS-232 and sent back to the BER test set. The data input to the test modulator is clocked at 6.25 KHz. This data is differentially encoded, level shifted to NRZ waveform, and sent to a mixer to biphase modulate a 70 MHz carrier. No prefiltering of the data is used for wave shaping prior to transmission. The differential encoder circuit is shown in Figure 3-30A. At the output of the test modulator facility is provided to inject noise for testing purpose.

3.3.2 Revised Demodulator and Data Decoder

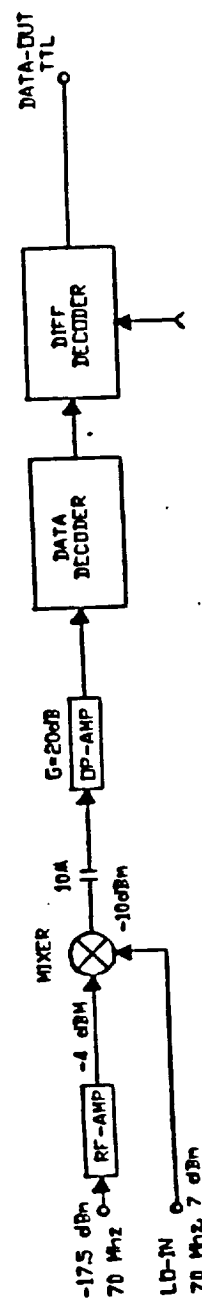
The BPSK demodulator is shown in Figure 3-29B. The input to this demodulator is the chirp transform pulses derived from the CMC processor. A carrier frequency (within 70 ± 5 MHz) is embedded in the pulses. For a single channel input these pulses occur at the repetition frequency of the chirp waveform. The relative phase of the carrier from pulse to pulse is determined by the data symbols. Since the signal is BPSK, the phase changes can only be 180° . An external CW signal which is at the same frequency and coherent to the BPSK signal carrier is mixed with the input chirp transform pulses. The result is a series of pulses at the output of the mixer, which are essentially the envelope of the chirp transform pulses. Depending on the current carrier phase the demodulated pulses are either positive or negative. As a result of the transmission system parameters defined earlier, the expected pulsewidth is approximately 200 nanoseconds. The demodulated pulses are detected in the data decoder to recover the differentially encoded data. This decoder is basically a threshold detector with adjustable positive and negative thresholds as shown in Figure 3-29B. Finally the data is recovered, by the differential decoder. The differential decoder circuit is shown in Figure 3-30B.

3.4 Close Loop BER Performance Test

Average BER performance of the satellite receiver is evaluated in the test set-up shown in Figure 3-31. A picture of the actual receiver under test is shown in Figure 3-32. In Figure 3-31 the satellite receiver, comprising the CMC processor, chirp waveform generator



(A) BPSK MODULATOR (TEST SOURCE)



(B) BPSK-DEMODULATOR

Figure 3-29:- (A) BPSK Modulator (Test Source). (B) BPSK-Demodulator

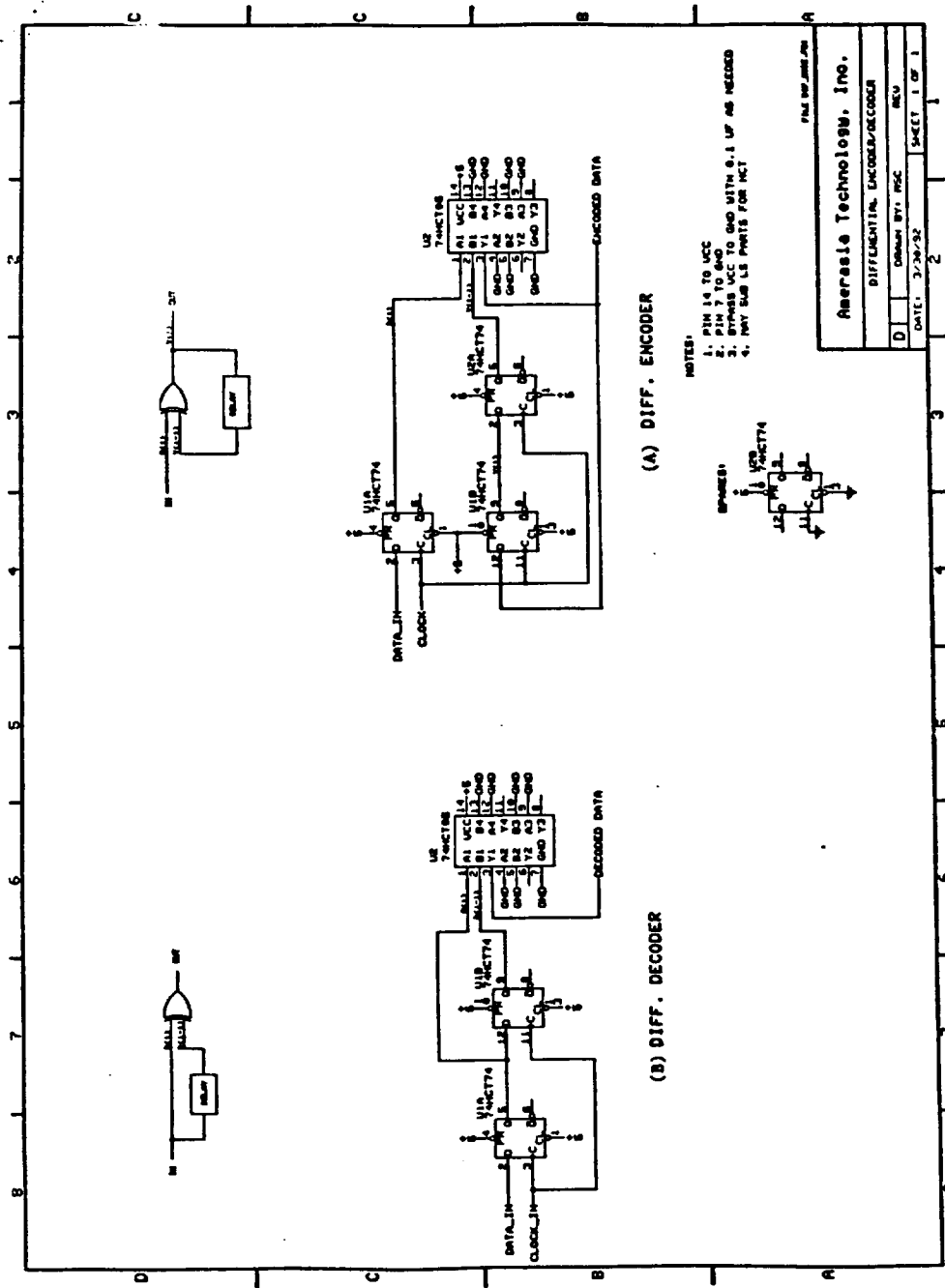


Figure 3-30:- (A) Differential Encoder. (B) Differential Decoder

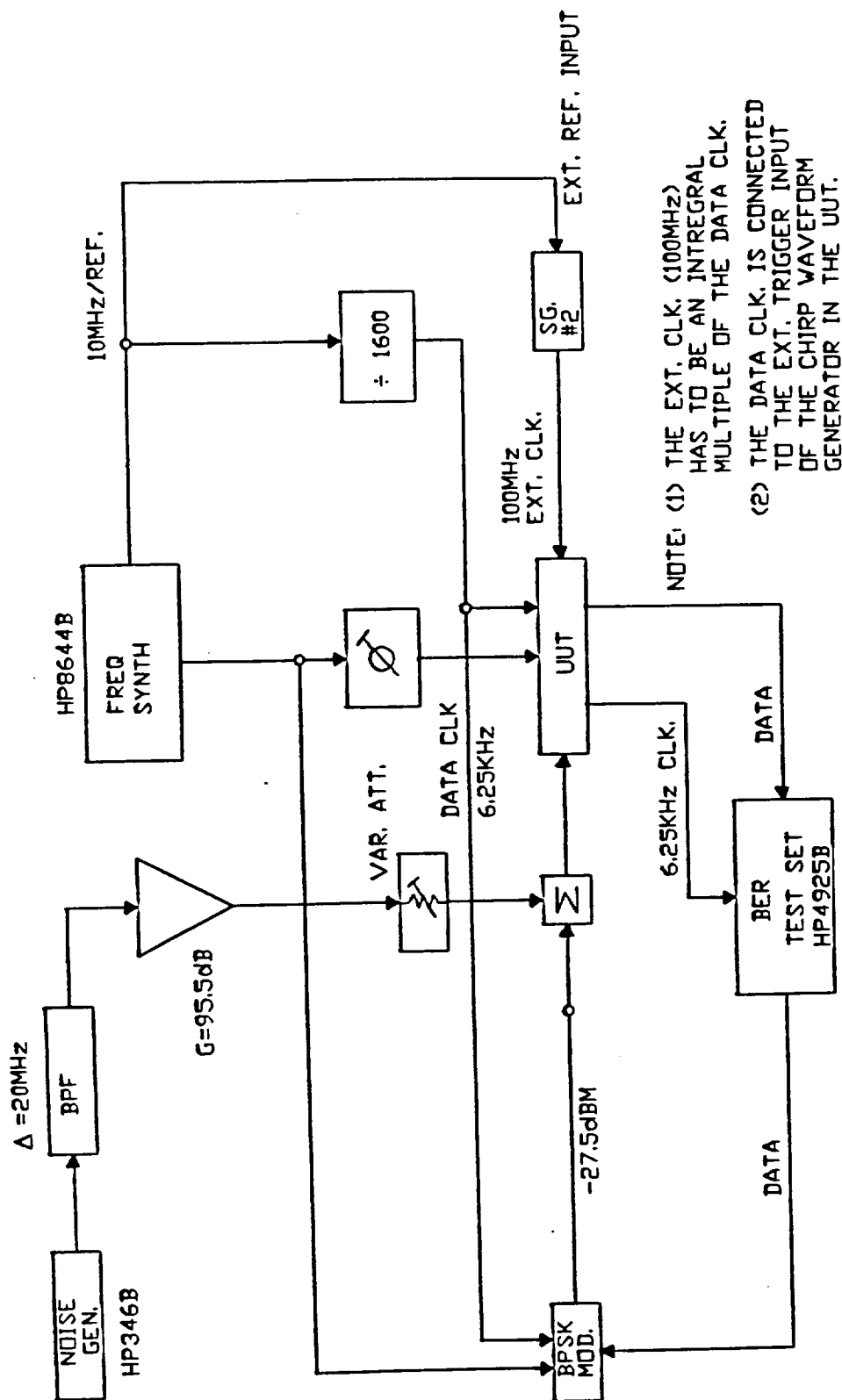


Figure 3-31:- Test Set-Up for Satellite Receiver Performance

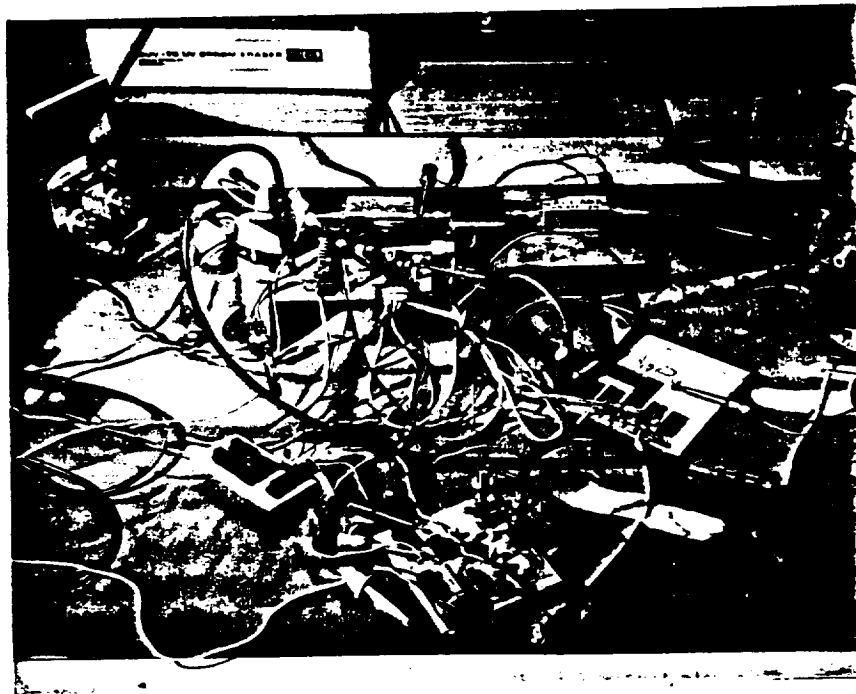


Figure 3-32:- Receiver Under Test

AMT-150, SSB modulator, and BPSK demodulator/decision circuit, is represented by the UUT (unit under test). Coherent demodulation is realized by driving the BPSK modulator (test source) and the BPSK demodulator with the same 70 MHz signal (from HP8644B) and by the adjustable phasemitter, as shown in the diagram. To maintain system timing integrity, data clock is derived from the internal reference 10 MHz frequency source of the frequency synthesizer (HP8644B). The data clock is generated by dividing this reference frequency by 1600 to obtain 6.25 KHz. This same clock signal is also used to control the chirp waveform repetition frequency of the AMT-250. For the same reason an external high frequency clock (100 MHz) signal, from a second signal generator, is injected into the AMT-250 for chirp waveform generation. This 100 MHz external clock is also phaselocked to the 10 MHz reference frequency. The exact characteristics of the baseband chirp waveform generated by the AMT-250 is given in Figure 3-33. Gaussian noise is added to the test signal from the BPSK modulator via a power combiner. This noise is bandlimited (20 MHz) by a bandpass filter. An HP346B diode noise generator is the primary source of noise, which is amplified to the desired level. The signal to noise ratio (S/N) selected for each

measurement is set by a variable attenuator. Taking into account the data bit rate of the transmitted data and the noise bandwidth, an equivalent E_b/N_0 is established for each S/N setting. The instrument used for BER measurements is an HP4925B BER test set. This instrument sends a repetitive PN-sequence, which is timed by the 6.25 KHz clock, to the BPSK modulator. The recovered data from the satellite receiver (UUT) is sent back to the BER test set for comparison.

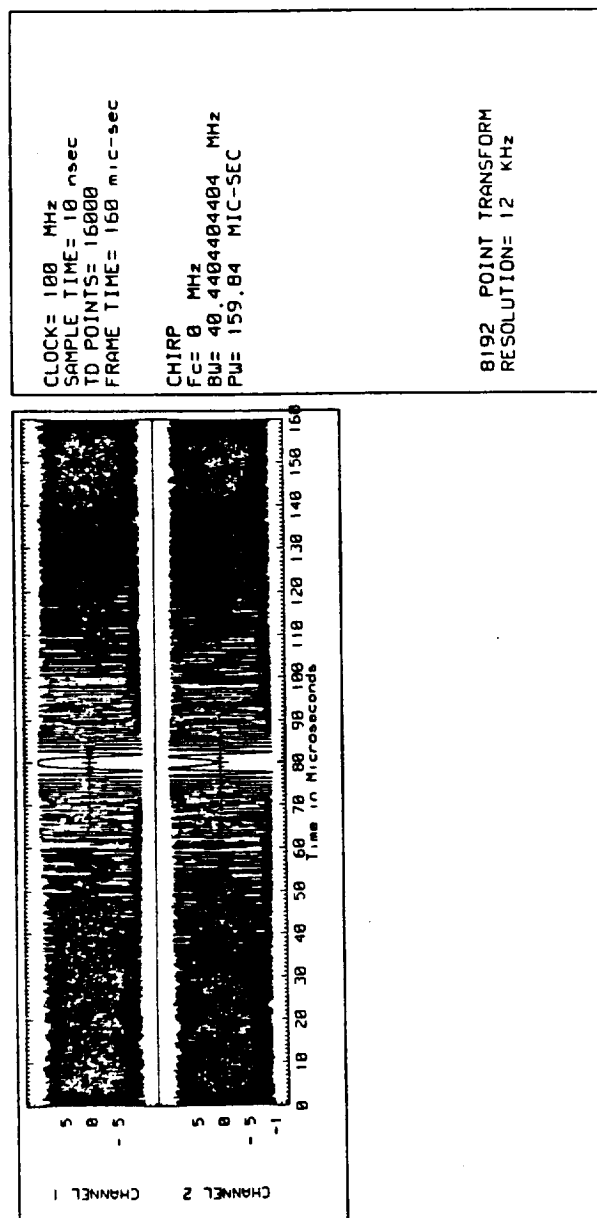
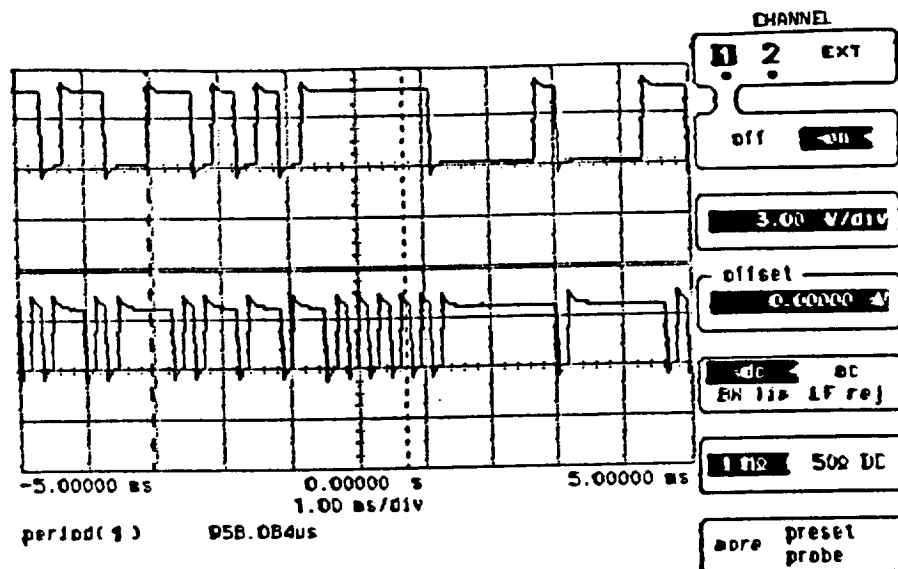


Figure 3-33:- Characteristics of Baseband Chirp Waveform From AMT-250

Prior to BER measurements major signal characteristics at various point of the system is recorded. In Figure 3-34 the transmitted data is shown before and after differential encoding. This picture demonstrates the accuracy of the encoding circuit.



	Sensitivity	Offset	Probe	Coupling
Channel 1	3.00 V/div	0.00000 V	10.00 :1	dc (1M ohm)
Channel 2	3.00 V/div	0.00000 V	10.00 :1	dc (1M ohm)

Trigger mode : Edge
 On Positive Edge Of Chan2
 Trigger Level
 Chan2 = 312.500 mV (noise reject OFF)
 Holdoff = 40.000 ns

Figure 3-34:- Transmitted Data Pattern

Figure 3-35A and B shows the relative phase change of the 70 MHz carrier signal from the BPSK modulator at the data transitions. The frequency spectrum of the BPSK signal centered around 70 MHz is shown in Figure 3-36.

Figures 3-37A and B show the output of the CMC processor, which is the chirp transform of the BPSK modulated signal. Figure 3-37A shows a state of the data symbol where the chirp transform carrier is out of phase (180°) with the reference carrier (upper trace) going into the BPSK demodulator, while Figure 3-37B shows the opposite situation. Figures

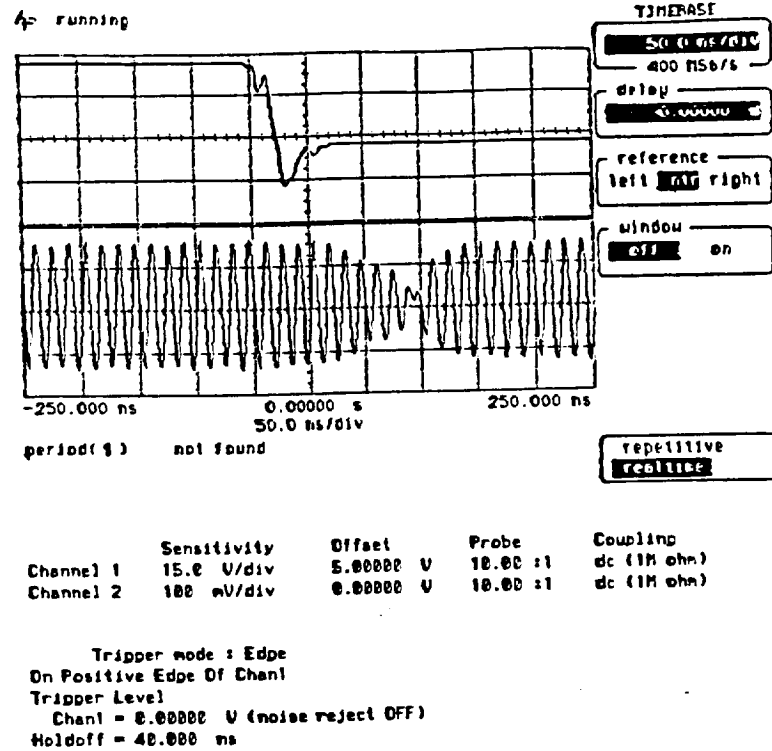


Figure 3-35A:- Waveform of BPSK Signal Showing Negative Data Transition

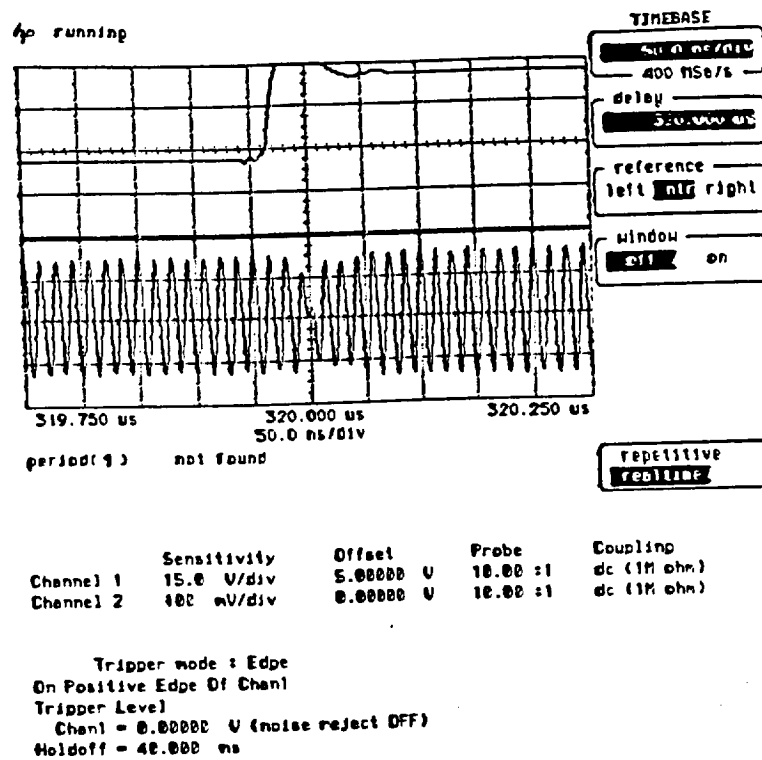


Figure 3-35B:- Waveform of BPSK Signal Showing Positive Data Transition

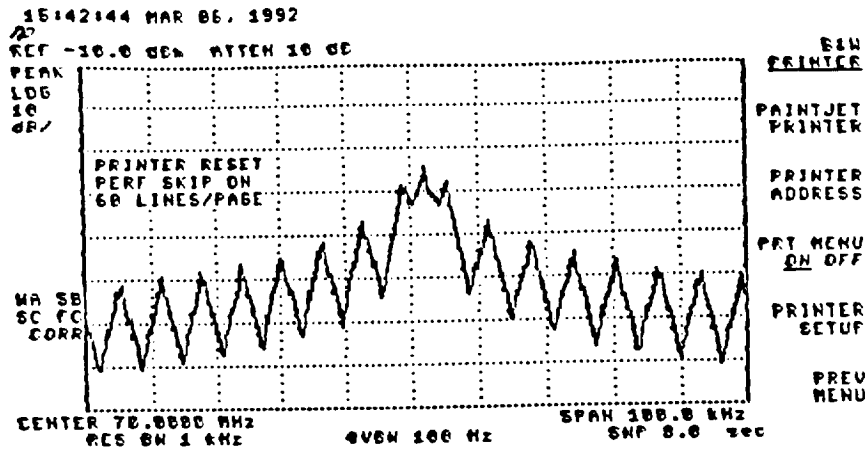
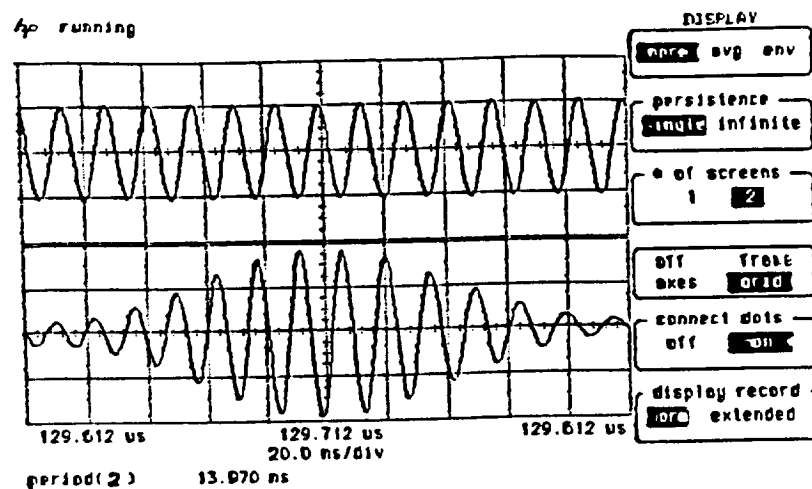


Figure 3-36:- Frequency Spectrum of BPSK Signal



	Sensitivity	Offset	Probe	Coupling
Channel 1	400 mV/div	0.00000 U	1.000 :1	dc (50 ohm)
Channel 2	4.00 U/div	0.00000 U	10.00 :1	dc (1M ohm)

Trigger mode : Edge
 On Positive Edge Of Ext1
 Trigger Level
 Ext1 = 1.31250 U (noise reject OFF)
 Holdoff = 48.000 ns

Figure 3-37A:- Output Waveform of CMC Processor

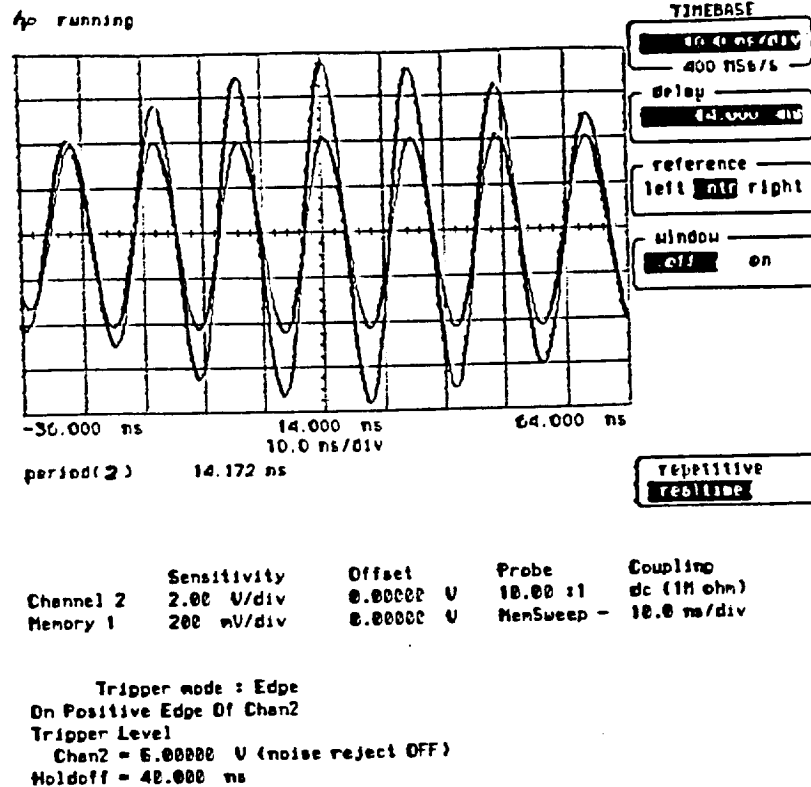


Figure 3-37B:- Output Wwaveform of CMC Processor

3-38A and B show the BPSK demodulator output waveform when the reference carrier is in-phase and out of phase with the chirp transform carrier. These figures clearly show the familiar $\sin X/X$ shape.

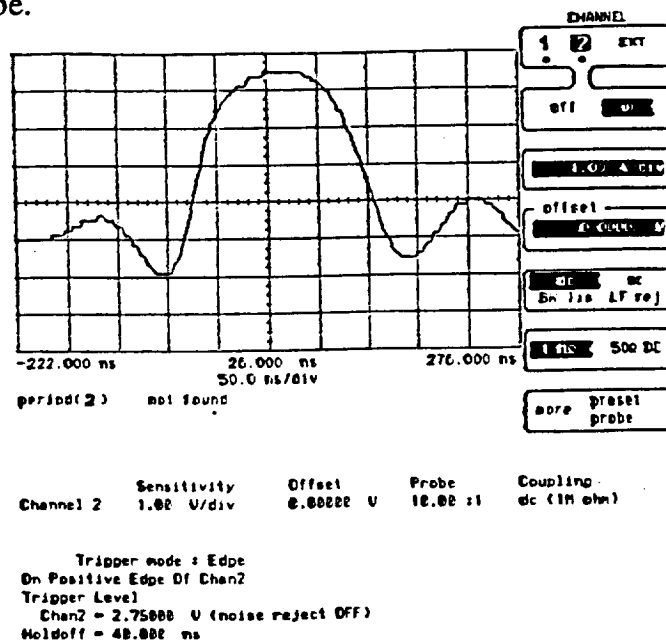


Figure 3-38A:- Output Waveform of BPSK Demodulator

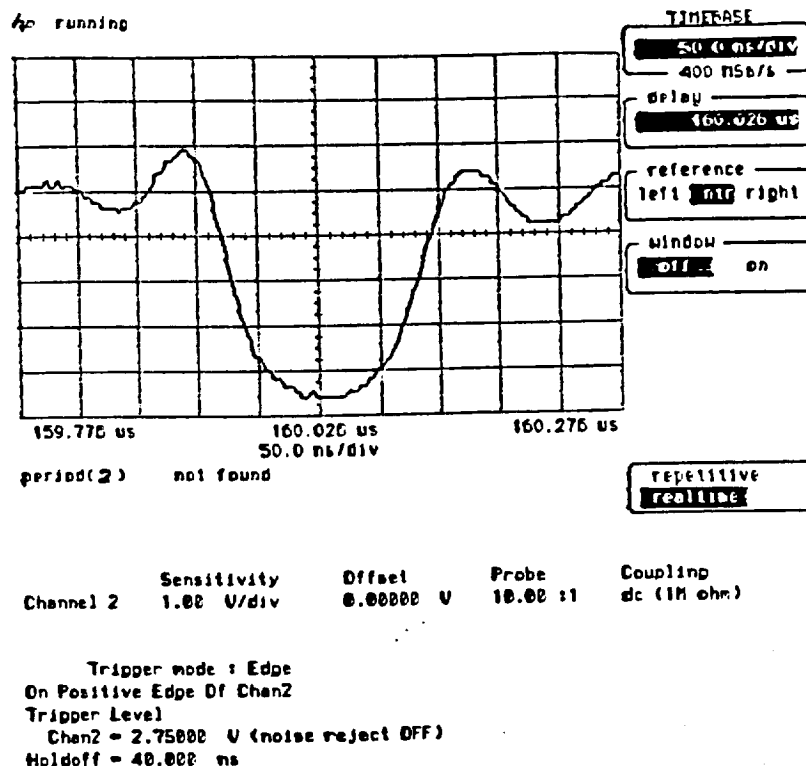
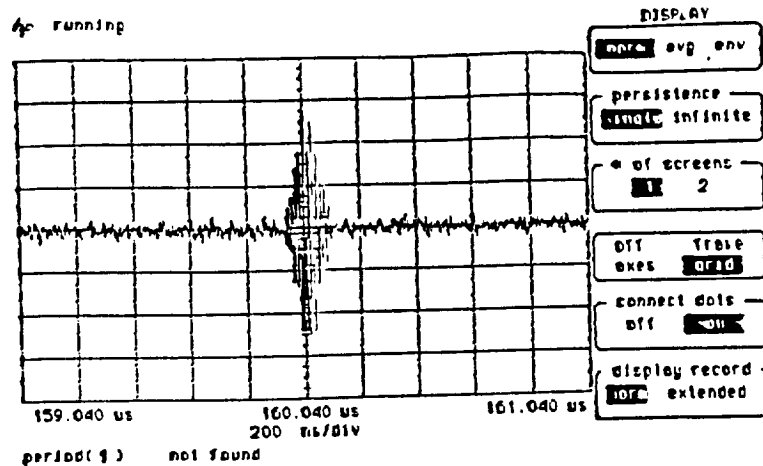


Figure 3-38B:- Output Waveform of BPSK Demodulator.

The output of the CMC processor with suppressed sidelobes are shown in Figures 3-39A, B, and C, displayed with various timebases of the oscilloscope to demonstrate alternate views of the transformed waveform.

The demodulated output of these transform pulses are shown in Figures 3-40A and 3-40B corresponding to the detected data symbol "1" and "0" respectively. The decision thresholds for data "1" and "0" are shown with respect to the demodulated transform pulses in Figures 3-41A and B. The thresholds are adjustable and for this measurement they are set at midpoints between the peak of the pulse and the highest peak of the sidelobes.

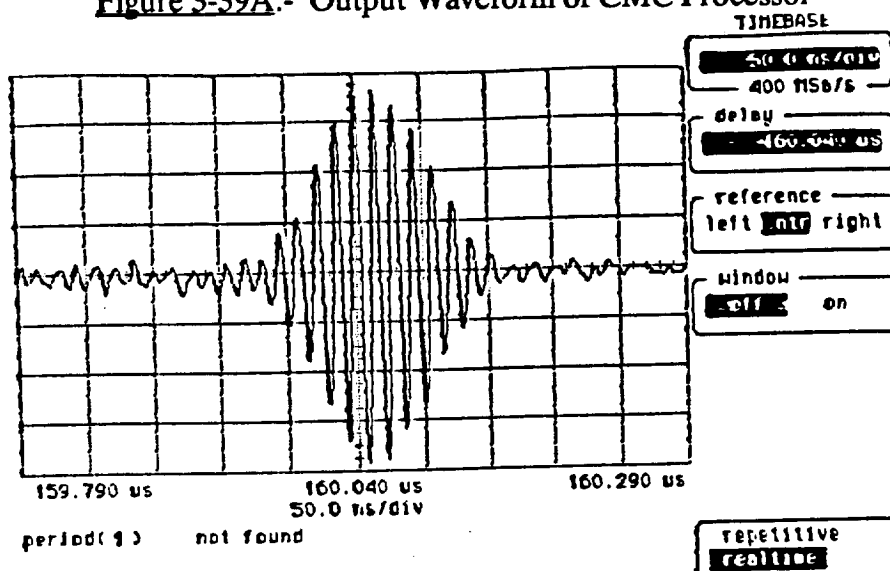
In an analysis conducted during the Phase II program it was concluded that the output carrier frequency of a CMC processor is constant regardless of the input frequency. This conclusion was made by neglecting frequency related terms in the close form solution of the chirp transform, due to an erroneous assumption that they were negligible. During the test, to verify this result, the error was discovered experimentally. By reinspecting the previously obtained theoretical result both experimental and theoretical results are in agreement,



	Sensitivity	Offset	Probe	Coupling
Channel 2	50.0 mV/div	0.00000 V	10.00 ±1	dc (1M ohm)

Trigger mode : Edge
 On Positive Edge Of Chan2
 Trigger Level
 Chan2 = 50.000 mV (noise reject OFF)
 Holdoff = 40.000 ns

Figure 3-39A:- Output Waveform of CMC Processor

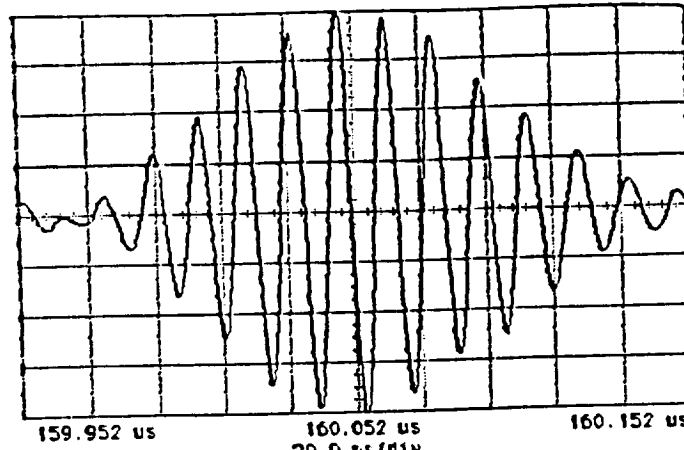


	Sensitivity	Offset	Probe	Coupling
Channel 2	50.0 mV/div	0.00000 V	10.00 ±1	dc (1M ohm)

Trigger mode : Edge
 On Positive Edge Of Chan2
 Trigger Level
 Chan2 = 50.000 mV (noise reject OFF)
 Holdoff = 40.000 ns

Figure 3-39B:- Output Waveform of CMC Processor.

4p stopped



TIMEBASE

20.0 ns/div

400 ns/s

delay

160.052 us

reference

left ☒ right

window

☒ on

period(1) not found

repetitive

realtime

Channel 2	Sensitivity	Offset	Probe	Coupling
	50.0 mV/div	0.00000 V	10.00 :1	dc (1M ohm)

Trigger mode : Edge

On Positive Edge Of Chan2

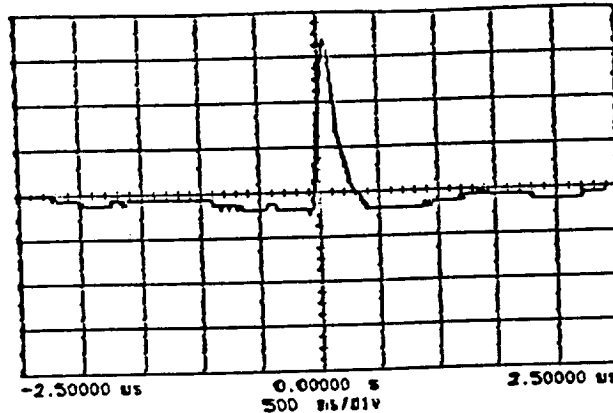
Trigger Level

Chan2 = 50.000 mV (noise reject OFF)

Holdoff = 40.000 ns

Figure 3-39C:- Output Waveform of CMC Processor

4p running



TIMEBASE

500 ns/div

100 ns/s

delay

0.00000 s

reference

left ☒ right

window

☒ on

period(1) not found

repetitive

realtime

Channel 2	Sensitivity	Offset	Probe	Coupling
	300 mV/div	0.00000 V	10.00 :1	dc (1M ohm)

Trigger mode : Edge

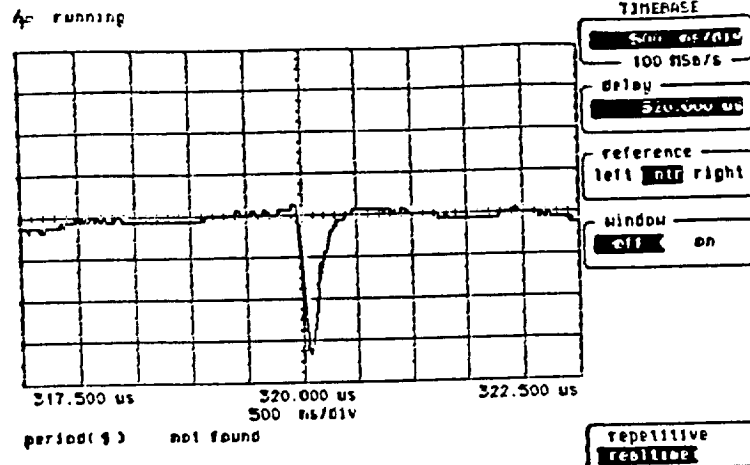
On Positive Edge Of Chan2

Trigger Level

Chan2 = 500.000 mV (noise reject OFF)

Holdoff = 40.000 ns

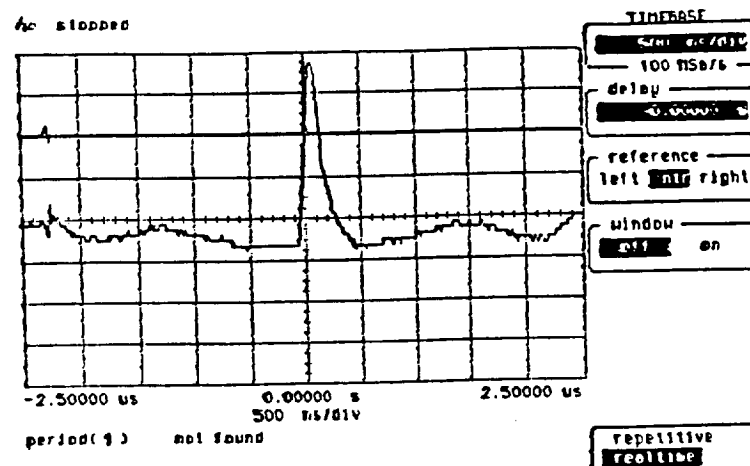
Figure 3-40A:- Demodulated Transform Pulse



	Sensitivity	Offset	Probe	Coupling
Channel 2	300 mV/div	0.00000 V	10.00 :1	dc (1M ohm)

Trigger mode : Edge
 On Positive Edge Of Chan2
 Trigger Level
 Chan2 = 500.000 mV (noise reject OFF)
 Holdoff = 40.000 ns

Figure 3-40B:- Demodulated Transform Pulse



	Sensitivity	Offset	Probe	Coupling
Channel 1	250 mV/div	0.00000 V	10.00 :1	dc (1M ohm)
Channel 2	250 mV/div	0.00000 V	10.00 :1	dc (1M ohm)

Trigger mode : Edge
 On Positive Edge Of Chan2
 Trigger Level
 Chan2 = 437.500 mV (noise reject OFF)
 Holdoff = 40.000 ns

Figure 3-41:- (A) Decision Thresold for Positive Transform Pulse

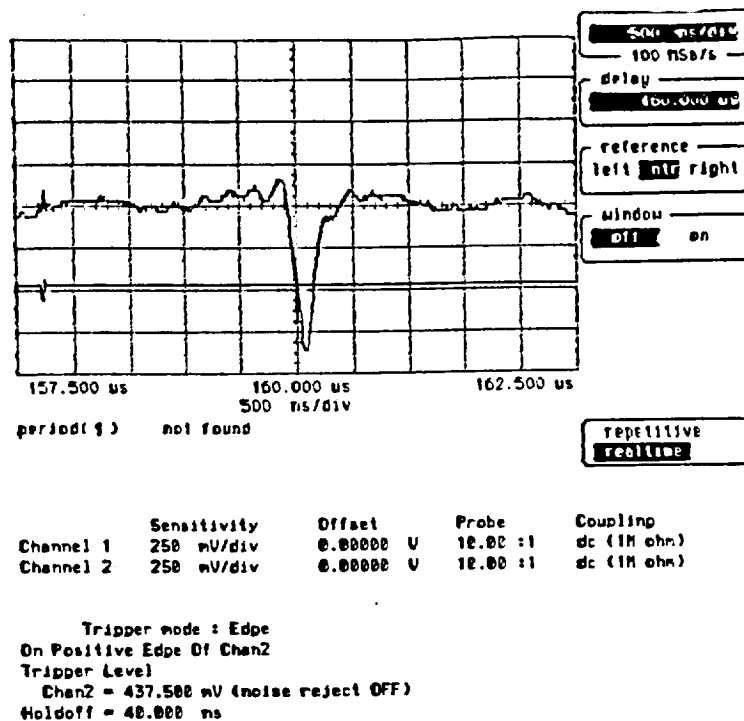
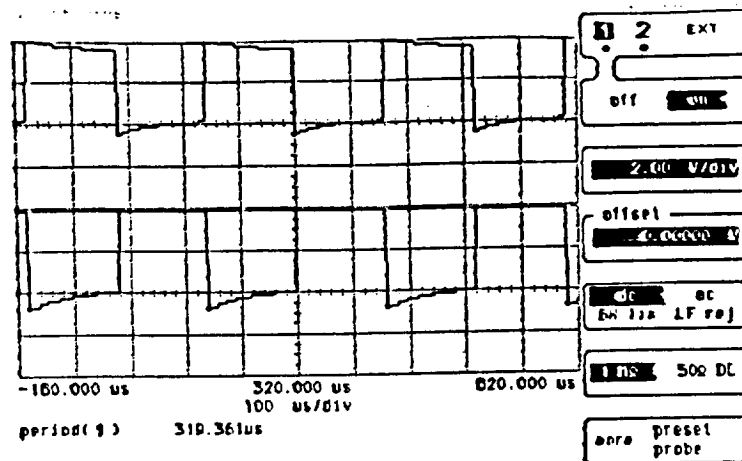


Figure 3-41:- (B) Decision Threshold Setting for Negative Transform Pulse

when those frequency terms are included. The theoretical correction is included in the this report's appendix. In Figure 3-42 the data transmitted is alternated between "1" and "0". The upper trace is the transmitted data, and the lower trace is the received data, which is a replica of the former. In this test the BPSK signal carrier frequency is changed to 71 MHz from 70 MHz. To demodulate the chirp transform pulses, a 71 MHz reference carrier must be injected into the BPSK demodulator. The resulting transform pulses are shown in Figures 3-43A and B, for positive and negative going pulses respectively. This is proof that the output carrier frequency of the CMC processor is also 71 MHz. The recovered data is shown in lower trace of Figure 3-42. Figures 3-44A through C show the results of identical experiments conducted with the input frequency set at 71.6 MHz.

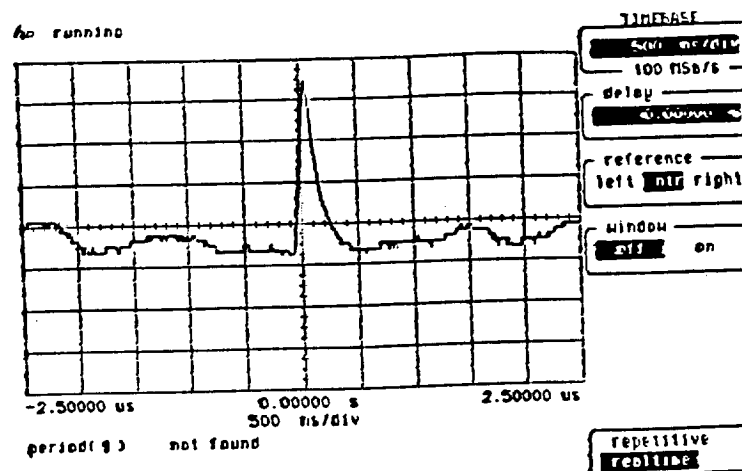
The BER measurement results are shown in Figure 3-45. Comparing these results with the theoretical BER performance curve^[2] versus S/N is shown in Figure 3-46. By comparing the theoretical and measured BER performance it is clear that the measured Figure 3-41A, Decision threshold setting for positive transform pulse.



	Sensitivity	Offset	Probe	Coupling
Channel 1	2.00 V/div	0.00000 V	10.00 s	dc (1M ohm)
Channel 2	2.00 V/div	0.00000 V	10.00 s	dc (1M ohm)

Tripper mode : Edge
 On Positive Edge Of Chan2
 Tripper Level
 Chan2 = 500.000 mV (noise reject OFF)
 Holdoff = 40.000 ns

Figure 3-42:- Data Output from Demodulator (Phase) After Reconstruction Utilizing the Chirp Transform Output Pulses. Upper Trace: Data Input to BPSK Modulator. Lower Trace: Data Output After Reconstruction. Input Frequency: 71 MHz. Phase Demodulator (Detector) LO Input Frequency: 71 MHz



	Sensitivity	Offset	Probe	Coupling
Channel 2	250 mV/div	0.00000 V	10.00 s	dc (1M ohm)

Tripper mode : Edge
 On Positive Edge Of Chan2
 Tripper Level
 Chan2 = 500.000 mV (noise reject OFF)
 Holdoff = 40.000 ns

Figure 3-43A:- Phase Detected Chirp Transform Output. Data Logic "1", (00). Input Signal Frequency: 71 MHz. Phase Detector LO Input Frequency: 71 MHz

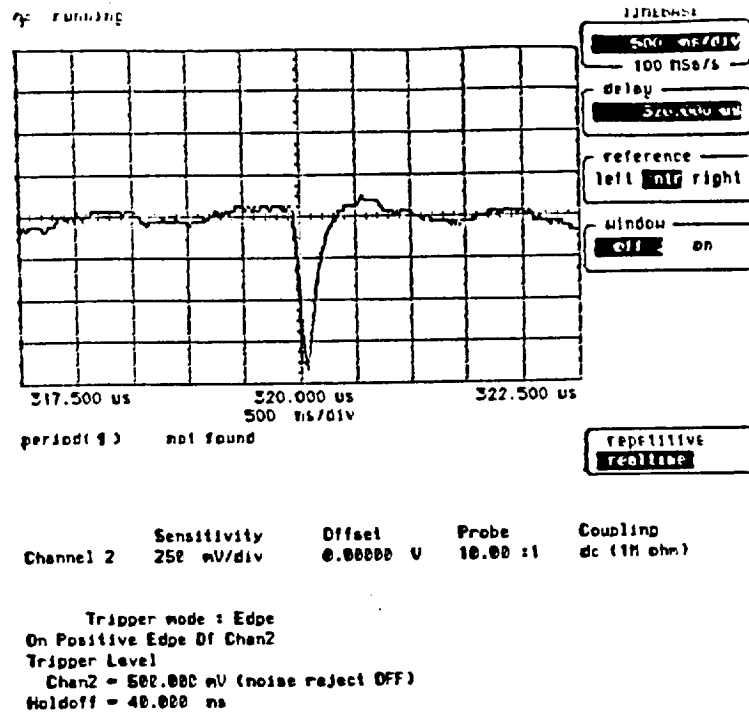


Figure 3-43B:-Phase Detected Chirp Transform Output. Data Logic "1", (180°). Input Signal Frequency: 71 MHz. Phase Detector LO Input Frequency: 71 MHz

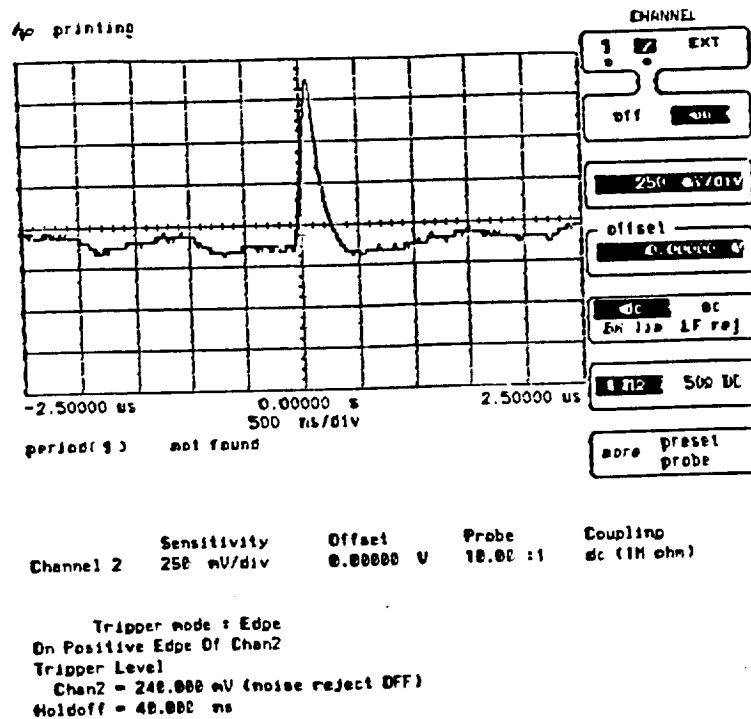


Figure 3-44A:-Phase Detected Chirp Transform Output. Data Logic "1", (0°). Input Signal Frequency: 71.6 MHz. Phase Detector LO Input Frequency: 71.6 MHz

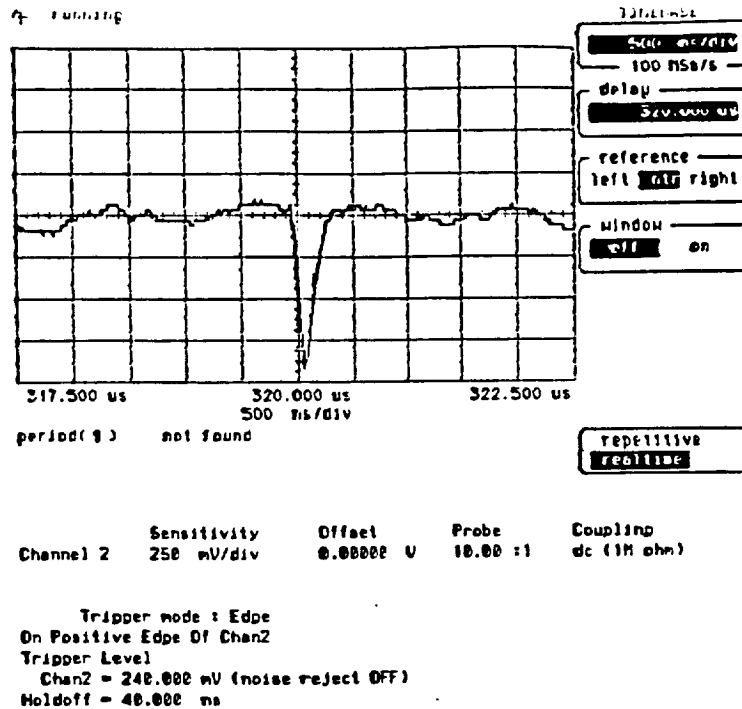


Figure 3-44B:- Phase Detected Chirp Transform Output. Data Logic "1", (180°). Input Signal Frequency: 71 MHz. Phase Detector LO Input Frequency: 71 MHz

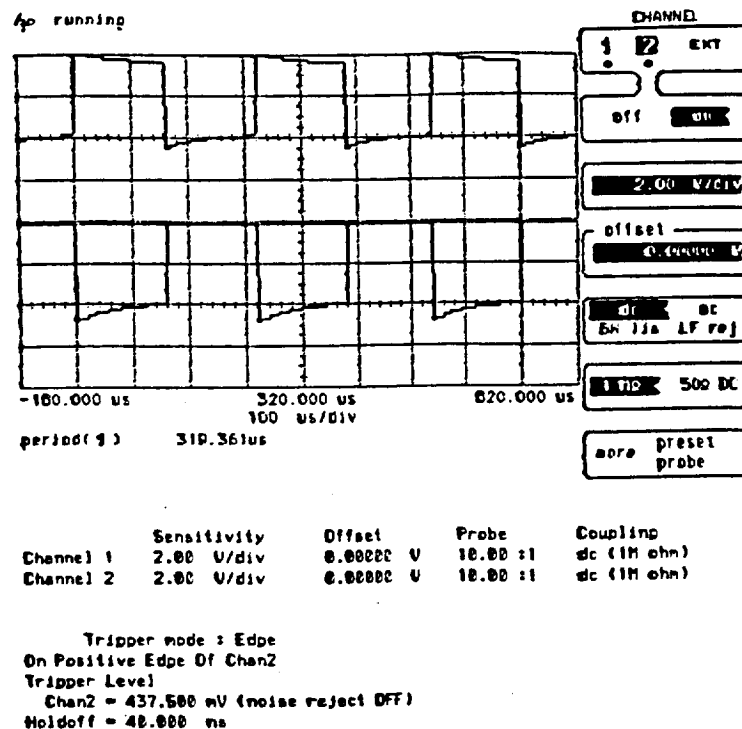


Figure 3-44C:- Data Output from Demodulator (Phase) After Reconstruction Utilizing the Chirp Transform Output Pulses. Upper Trace: Data Input to BPSK Modulator. Lower Trace: Data Output After Reconstruction. Input Frequency: 71.6 MHz. Phase Demodulator (Detector) LO Input Frequency: 71.6 MHz

result is approximately 10 dB worse than the theoretical curve. The difference is due to the decision process in determining whether the received symbol is a one or a zero. The theoretical performance curve is based on optimum sampling, where the demodulated pulses are sampled at its peak and compared to a decision threshold. In the experiment the demodulated pulses train are simply passed through a threshold detector. Each pulse is approximately 200 nanoseconds wide, occurring every 160 μsec . In every symbol interval the pulse is absent for approximately 159.8 μsec and the remainder of the repetition interval is filled with noise only. Therefore, during the absence of a pulse, the noise voltage peaks can still reach or exceed the threshold causing an erroneous decision, thus increasing the error probability. In the theoretical case the decision circuit looks at the pulse only once per symbol period, that is when the signal is present. Clearly, in the latter case, an erroneous decision can only be made during the presence of the demodulated pulse.

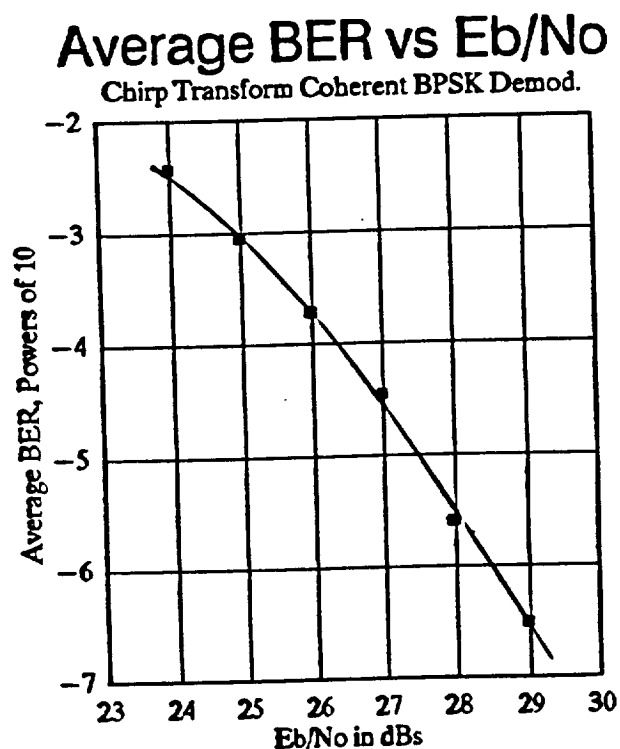


Figure 3-45:- BER Measurement As A Function of E_b/N_0

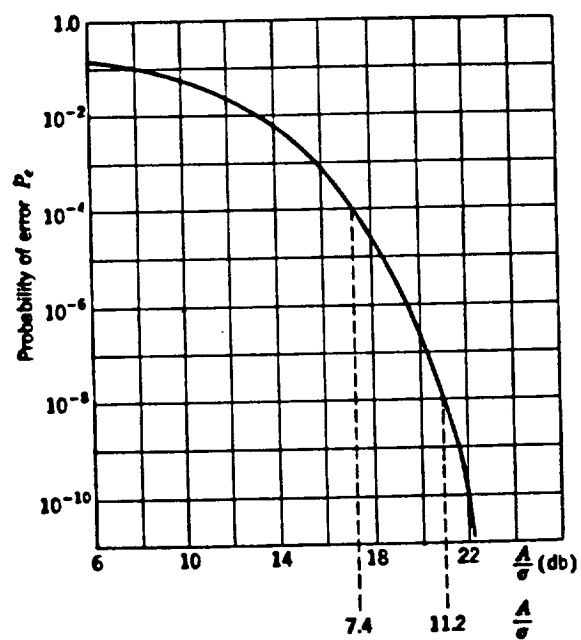


Figure 3-46:- Probability of Error for Binary Detection

3.5 Delivery Items:

The following softwares and hardwares, under this contract, will be delivered:

- 1) HIRAC Design Software.
- 2) Arbitrary Waveform Generator (Software, Hardware and Operating Mannual).
- 3) BPSK Demomulator and Modulator.
- 4) SSB Modulator.

4.0 CONCLUSIONS

The demodulation and detection of BPSK signals derived from a CMC chirp transform processor was experimentally demonstrated. The detection process had to be coherent in order to maintain good error rate performance. Although the experiment was conducted utilizing BPSK modulation, the detection technique applies also for QPSK modulation. The measured BER performance is 10 dB worse than theory, because the decision circuit was based on a simple threshold detector as opposed to optimum sampling each chirp transform pulse at the symbol rate. By synchronizing the chirp repetition clock to the data symbol timing, the data can easily be reconstructed from the chirp transform pulses. A technique to demodulate and detect QPSK signals are also given, but not demonstrated due to schedule and funding limitations.

The SAW filters in the CMC processor must be weighted to reduce time sidelobes, in order to reduce channel-to-channel spillover. In this experiment Taylor weighting was used, which provides 32 dB of sidelobe suppression. For satellite communications application major factors, such as symbol rate, channel separation, system synchronization, carrier synchronization, etc., have to be considered in the system design. The Phase II program has revealed how these factors have to be implemented and how they are interrelated.

5.0 References

1. Otto O.W., "Chirp Transform Signal Processor", Ultrasonic Symposium, 1976.
2. Schwarz M., "Information, Modulation, and Noise", 3rd edition, McGraw-Hill, 1980
3. Simon M.K., et al, "Multiple Symbol Differential Detection of MPSK", IEEE Trans. Comm., Vol. 38, March 1990.
4. Spilker Jr. J.J., "Digital Communication by Satellite", Prentice-Hall, 1977.

6.0 APPENDICES

A1. THEORETICAL ANALYSIS OF THE CMC PROCESSOR

The model used for computer analysis of the CMC chirp transform process is shown in Figure A1-1. The input and output filters have an impulse response with a positive slope (i.e. up-chirp) as shown, where the rate of the linear frequency change is equal to $2k$. The chirp generator produces a linear frequency chirp that has a negative slope equal to $-2k$. It has been shown elsewhere^[1] that the time-bandwidth product of the input and output filters has to be identical (BT), while the chirp generator time-bandwidth product must be at least four times larger ($4BT$). Note that the input filter has an inherent characteristic of delaying high frequency signals more than low frequency signals.

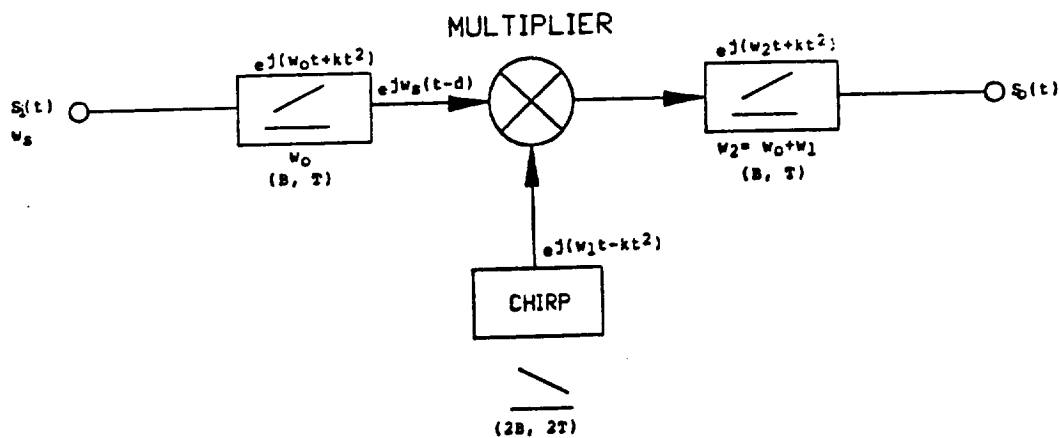


Figure A1-1:- Model of CMC Chirp Transformer

To generalize the analysis, the input signal is represented in complex form, as follows:

$$S_i(t) = e^{j\omega_s t} \quad (\text{A1-1})$$

The output of the input filter is delayed by d seconds, where d is dependent on the input frequency ω_s , hence

$$S_i(t-d) = e^{j\omega_s(t-d)} \quad (\text{A1-2})$$

$$d = (\omega_s - \omega_0)/2k \quad (\text{A1-3})$$

In the Multiplier, the product of the delayed input signal and the chirp signal is generated. This product is convolved with the impulse response of the output filter to produce the output signal $S_o(t)$, therefore,

$$S_o(t) = \int_{-T/2}^{T/2} x(t).y(t).h_2(\tau-t) d(\tau) \quad (\text{A1-4})$$

For $0 \leq \tau \leq T/2$

Where, $x(t)$ is given by (A1-2), and $y(t)$ and $h_2(t)$ are as follows,

$$y(t) = \text{Exp}[j(\omega_1 t - kt^2)] \quad (\text{A1-5})$$

$$h_2(t) = \text{Exp}[j(\omega_2 + kt^2)] \quad (\text{A1-6})$$

Since the input signal $S_i(t)$ is complex, the output, $S_o(t)$, of the processor is also complex. In this analysis, only the real part of $S_o(t)$ is considered. It can be shown that,

$$R_e[S_o(t)] = \text{Cos}[-\omega_s d + \omega_2 \tau + k\tau^2 + k\epsilon \tau] x(T-\tau) (\text{Sinc } q) \quad (\text{A1-7})$$

Where,

$$\text{Sinc } q = (\text{Sin } q)/q$$

$$q = [(\omega_s + \omega_1 - \omega_2 - 2k\tau)(T-\tau)/2]$$

ϵ is defined as,

$$\epsilon = \tau - (\omega_s + \omega_1 - \omega_2)/2k \quad (\text{A1-8})$$

$\omega_s, \omega_0, \omega_1$, and ω_2 , are as defined in Figure A1-1.

Based on the above model, a computer analysis is performed to demonstrate the transform output of a CW input signal. The CMC chirp transform parameters used for this

purpose are as follows:

Input frequency: $f_s = 100 \text{ MHz}$

$$\omega_s = 2\pi f_s$$

Center frequency of input filter:

$$f_o = 100 \text{ MHz}$$

Center frequency of output filter:

$$f_2 = 300 \text{ MHz}$$

Center frequency of the chirp:

$$f_1 = 200 \text{ MHz}$$

Time-Bandwidth product of the input and output filters is:

$$BT = 512$$

Time-Bandwidth product of the chirp generator is:

$$4BT = 2048$$

The chirp slope is: $2k = 4.2 \times 10^6 \pi \text{ Mrad/second}$

As can be seen from equations (A1-3) and (A1-8), when the input frequency f_s is equal to f_o , $d = 0$, and $\epsilon = \tau$. The computer analysis result is shown in Figure A1-2. The output frequency is 300 MHz, and the envelope of the waveform is a $(\sin x)/x$ function as is given by (A1-7). The width of the mainlobe (null-to-null) is approximately 60 nanoseconds, and the peak of the largest sidelobe is 13.5 dB below the main peak as expected from the $(\sin x)/x$ characteristic. In a multichannel communications system the sidelobes must be suppressed to prevent adjacent channel interference. For that purpose a weighting function can be designed into the SAW chirp filter. In what follows, sidelobe reduction is demonstrated by utilizing Hamming weighting.

To reduce the sidelobes of the chirp transform output, Hamming weighting can be incorporated in the SAW dispersive filter or in the chirp generator. In practice the basic chirp waveform is generated by a software controlled digital circuit. Therefore, it is easier to incorporate the weighting function in the chirp generator, hence the analysis is done with

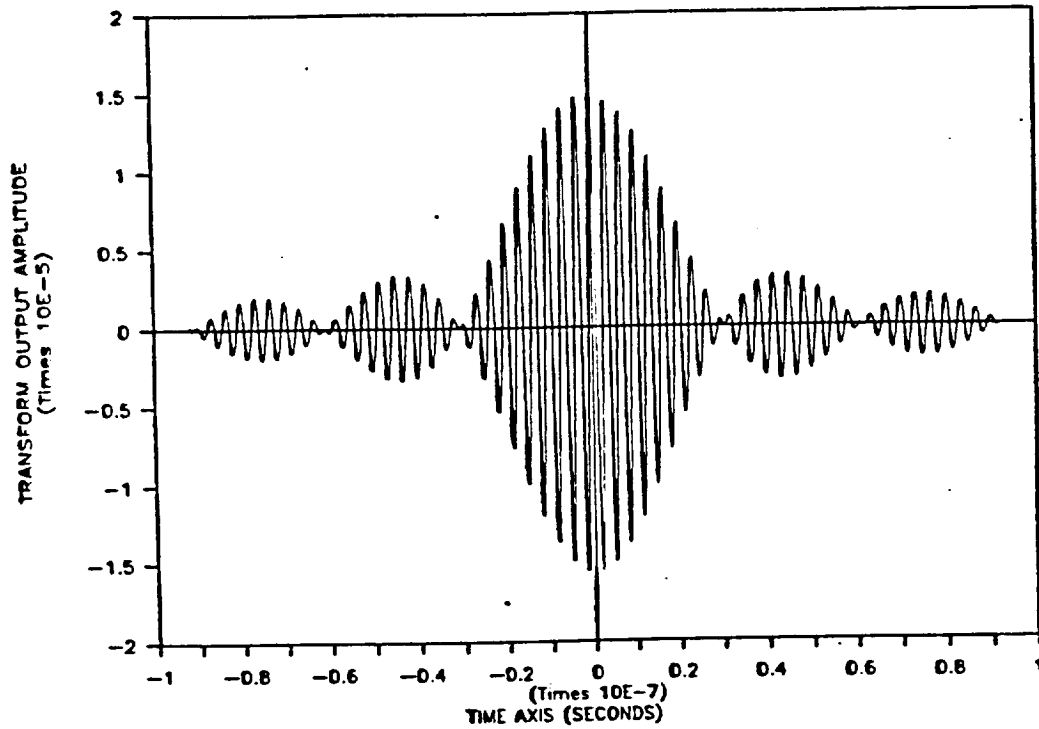


Figure A1-2:- Ideal CMC Transform Output

a weighted chirp waveform from the chirp generator. The generalized Hamming[.] weighting function is given by:

$$W(t) = a + (1-a)\cos(\pi t/T) \quad \text{for } -T \leq t \leq T \quad (A1-9)$$

$$W(t) = 0 \quad \text{otherwise.} \quad 0 \leq a \leq 1$$

In complex form, the chirp function becomes:

$$y(t) = a \cdot \exp[j(\omega t - kt^2)] + [(1-a)/2] \{ \exp[j(\omega + \pi/T)t - kt^2] + \exp[j(\omega - \pi/T)t - kt^2] \} \quad (A1-10)$$

The chirp transform output, $S_{Oh}(t)$, with Hamming weighting is obtained by replacing the chirp function $y(t)$ in (A1-4) by (A1-10). By solving the resulting convolution integral equation and taking its real value, the transform output, for $0 \leq \tau \leq T/2$, is as follows:

$$R_e[S_{Oh}(t)] = a(T-\tau)\cos[-\omega_s d + (\omega_2 + k\epsilon)\tau + k\tau^2][\sin k\epsilon(T-\tau)]/k\epsilon(T-\tau) +$$

$$[(1-a)(T-\tau)/2]\cos[-\omega_s d + (\omega_2 - \pi/2T + k\epsilon)\tau + k\tau^2] X$$

$$\begin{aligned} & \{ \sin[(\pi/T - 2k\epsilon)(T-\tau)/2] \} / [(\pi/T - 2k\epsilon)(T-\tau)/2] + \\ & [(1-a)(T-\tau)/2] \cos[-\omega_s d + (\omega_2 + \pi/T + k\epsilon)\tau + k\tau^2] \times \\ & \{ \sin[(\pi/T + 2k\epsilon)(T-\tau)/2] \} / [(\pi/T + 2k\epsilon)(T-\tau)/2] \end{aligned} \quad (A1-11)$$

Utilizing the above model the performance of the CMC chirp transform is simulated, and the results shown in Figures A1-3, A1-4, A1-5, and A1-6. In Figure A1-3, the weighting coefficient, a , is set to 1, which is equivalent to no weighting. As expected the result is identical to Figure A1-2. Subsequently, " a " is given values of .4, .5, and .54, respectively, and the results are shown in Figures A1-4, A1-5, and A1-6. As can be seen, the sidelobes are reduced relative to the mainlobe when compared to the results in Figures A1-2 and A1-3. Note, however, that the mainlobe is also slightly reduced, depending on the value of the weighting coefficient. However, there are other weighting functions that produces better sidelobe

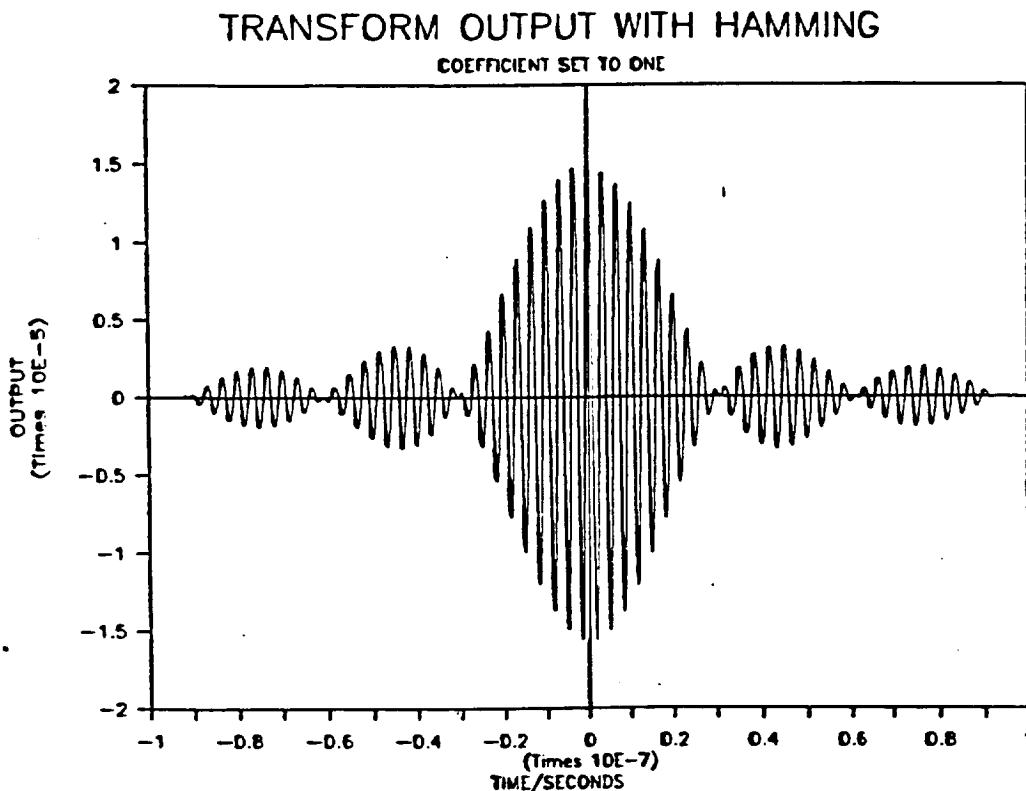


Figure A1-3:- Transform Output With Hamming (Coefficient Set to 1)

suppression, e.g. Taylor weighting.

By examining equation (A1-7), it can be shown that the output frequency of the CMC chirp transform is $\omega_2 + (\omega_s - \omega_0)/2 + 2k\epsilon$. At the center of the transform pulse $\epsilon = 0$, and the output frequency is $\omega_2 + (\omega_s - \omega_0)/2$. The phase response of the output carrier signal is:

$$\Phi(\omega_s) = [-\omega_s d] \text{ Rad.} \quad (\text{A1-12})$$

From (A1-3) and (A1-8), d and τ are as follows,

$$d = (\omega_s - \omega_0)/2k \quad (\text{A1-13})$$

$$\tau = (\omega_s - \omega_0)/2k + \epsilon \quad (\text{A1-14})$$

By substituting (A1-13) and (A1-14) into (A1-12), the phase response, $\Phi(\omega_s)$, is obtained and given by (A1-15).

$$\Phi(\omega_s) = -(\omega_s - \omega_0)[-\omega_s/k] \text{ radians} \quad (\text{A1-15})$$

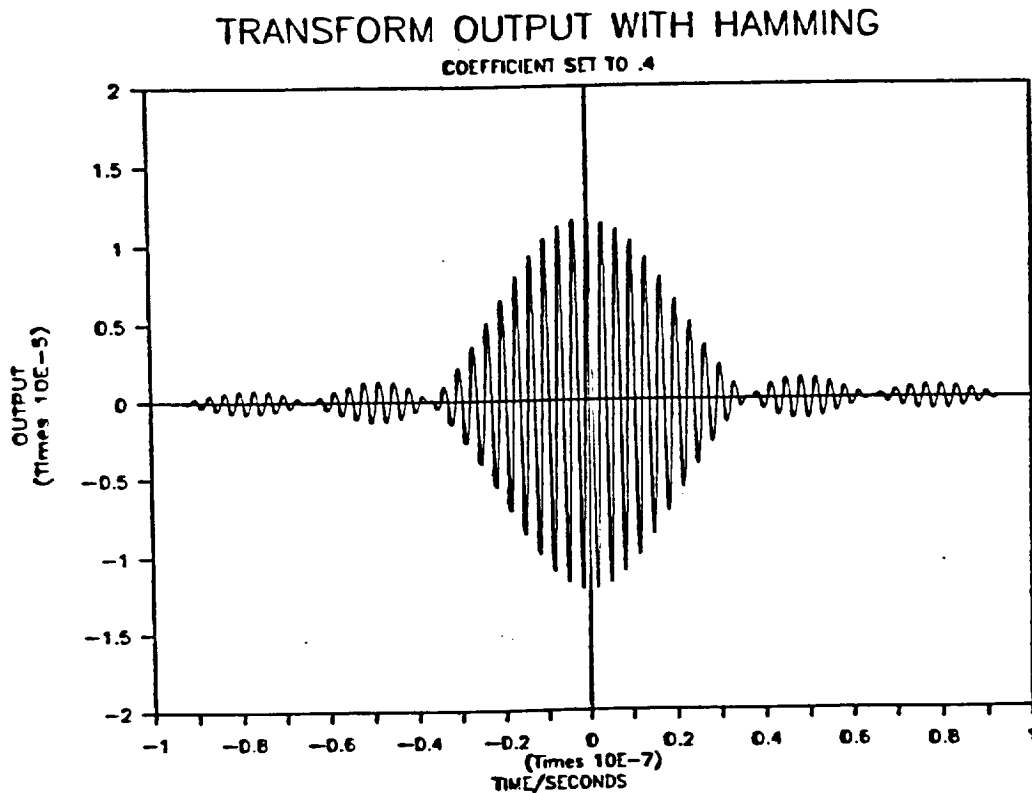


Figure A1-4:- Transform Output With Hamming Weighting (Coefficient Set to 0.4)

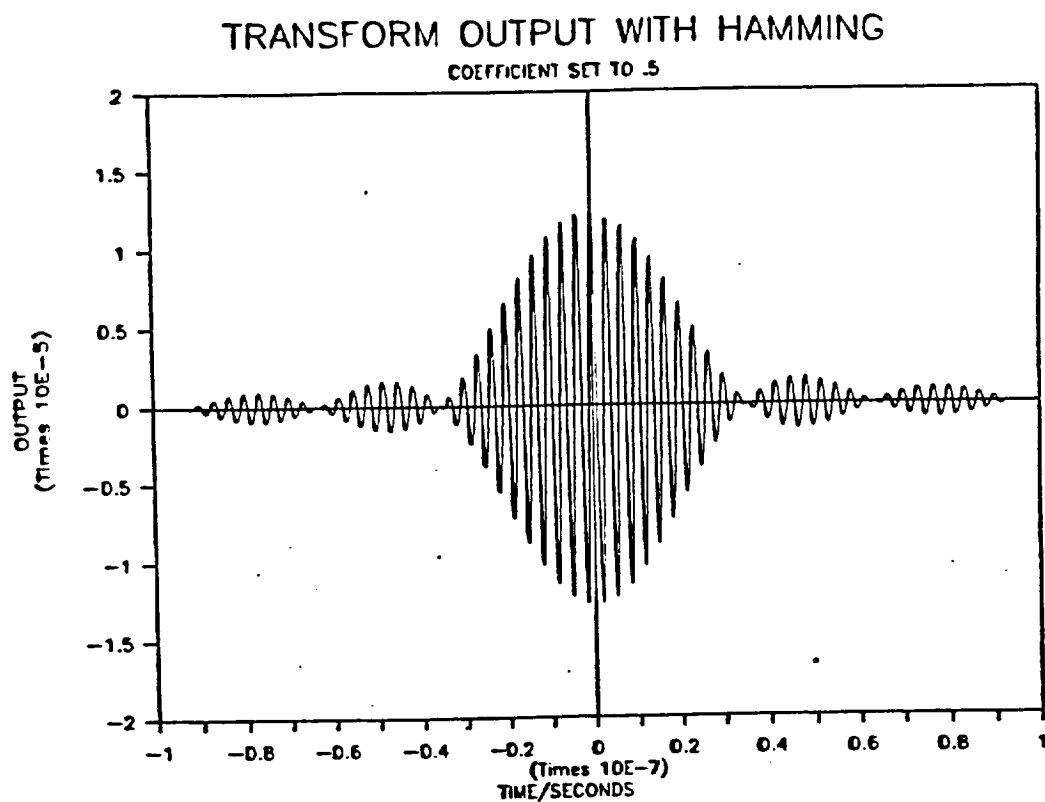


Figure A1-5:- Transform Output with Hamming (Coefficient Set to 0.5)

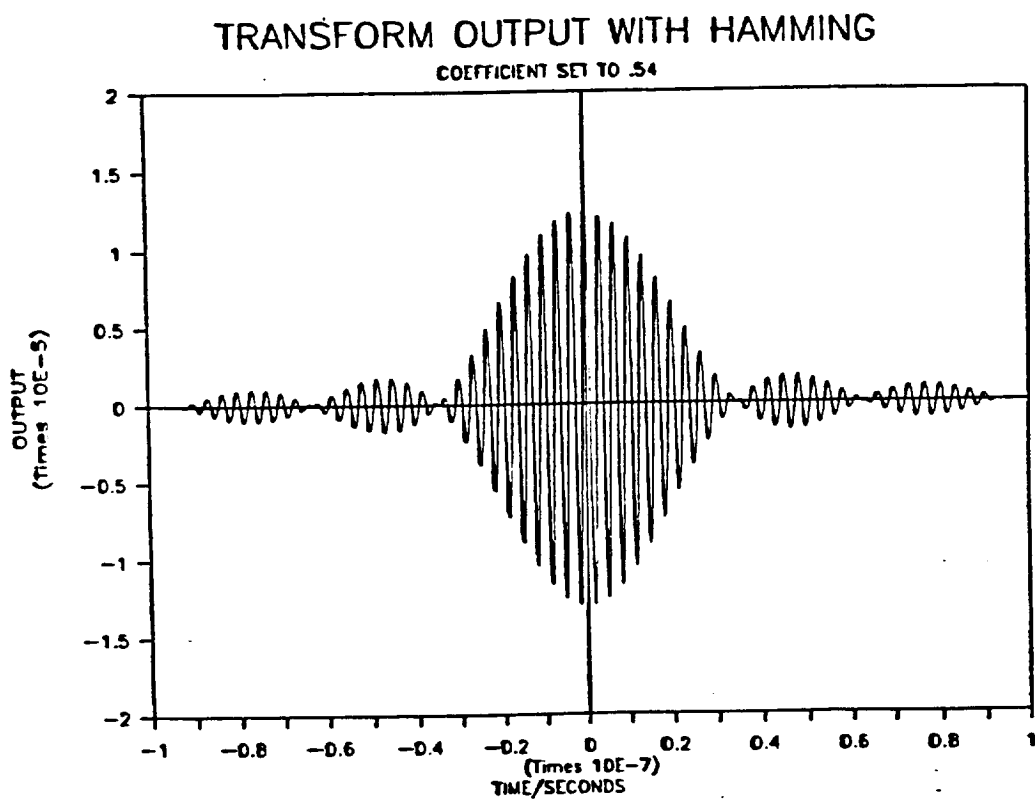


Figure A1-6:- Hamming Output with Hamming (Coefficient Set to 0.54)

A2. EXPERIMENTAL RESULTS

To verify the theoretical results described above, an experimental circuit was built using existing dispersive SAW filters. The circuit used for this experiment is shown in Figure A2-1, and the test set-up is shown in Figure A2-2. The dispersive SAW filters have the following characteristics:

Center frequency: 70 MHz
Bandwidth (40 dB): 20 MHz
Weighting function: Taylor
Chirp slope: .253 MHz/ μ second
Time delay: 80 microseconds

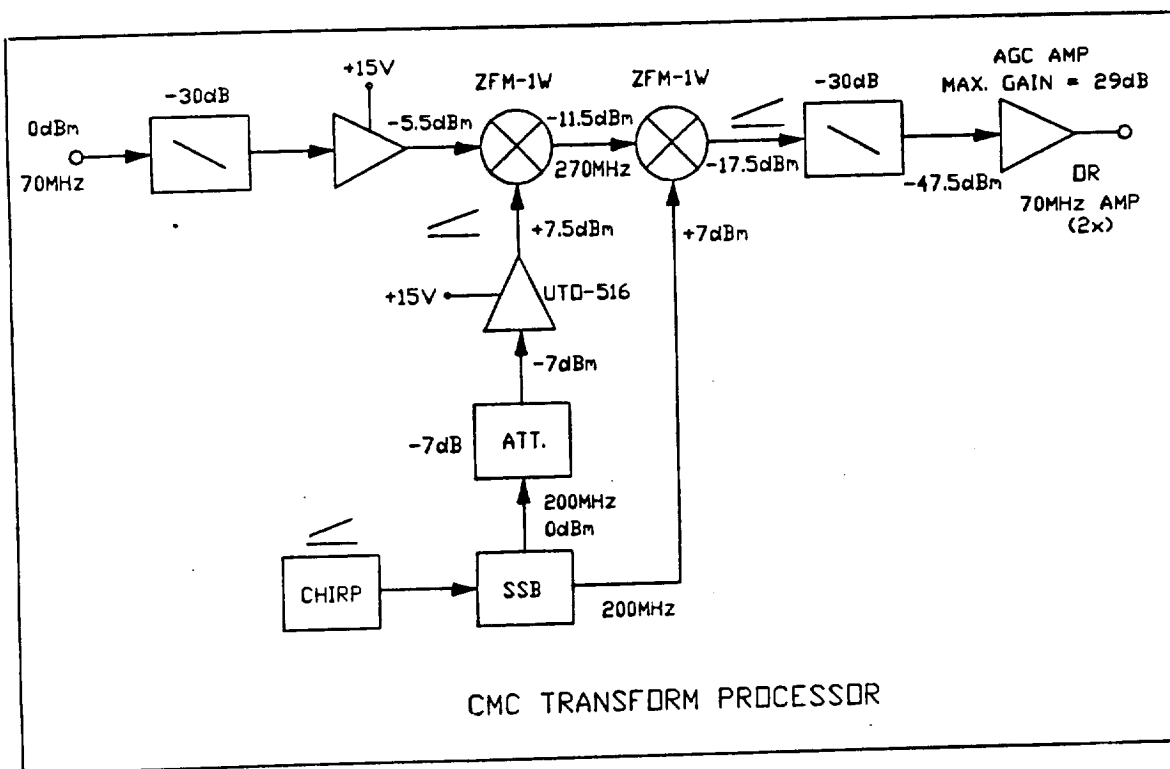


Figure A2-1:- CMC Transform Processor

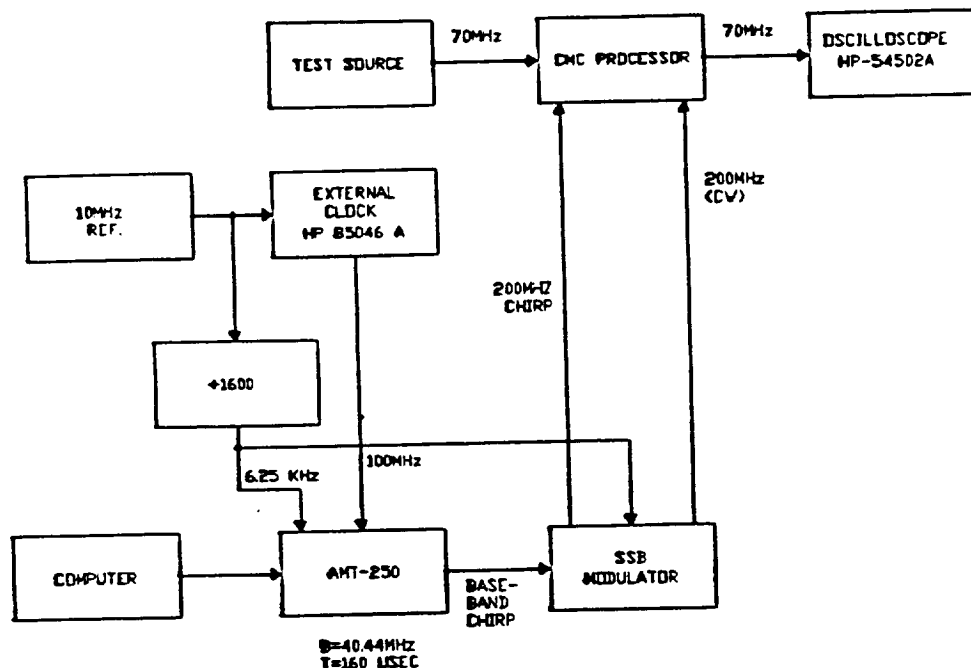


Figure A2-2:- Test Set-Up for CMC Transform Processor

Because both SAW filters operate at the same frequency, frequency conversions have to be incorporated to construct the CMC processor so that its input and output center frequencies are the same. This is accomplished by the two mixers, ZFM-1W, shown in Figure A2-1. The chirp waveform generator and SSB modulator were developed for the NASA/LEWIS SBIR Contract No. NAS3-25862. The output chirp waveform of the SSB modulator is measured utilizing Hewlett Packard's 400 Msample/second digital oscilloscope, and the result is shown in Figure A2-3. In this diagram only the center part of the chirp is shown, because of limited resolution of the plotter to cover the entire period of the chirp. The chirp waveform was adjusted to be the same as the SAW filter chirp slope, i.e. .253 MHz/ μ second, and the chirp period is approximately 90 μ seconds. Since the Time-bandwidth product of the chirp generator has to be four times the SAW filter's, only the center region of the dispersive filter's passband is used to obtain a proper transform output.

Initially, the input frequency is tuned to 70MHz and the CMC processor output waveform is plotted as shown in Figure A2-4. As expected the output frequency is also 70 MHz.

Subsequently, the input frequency is changed to 70.0015 MHz, and the output waveform is recorded and shown in Figure A2-5. The output phase dependency on input frequency implies that in order to obtain coherent demodulation of phase modulated signals, the carrier phase tracking circuit has to take into account the phase shift introduced by the CMC processor.

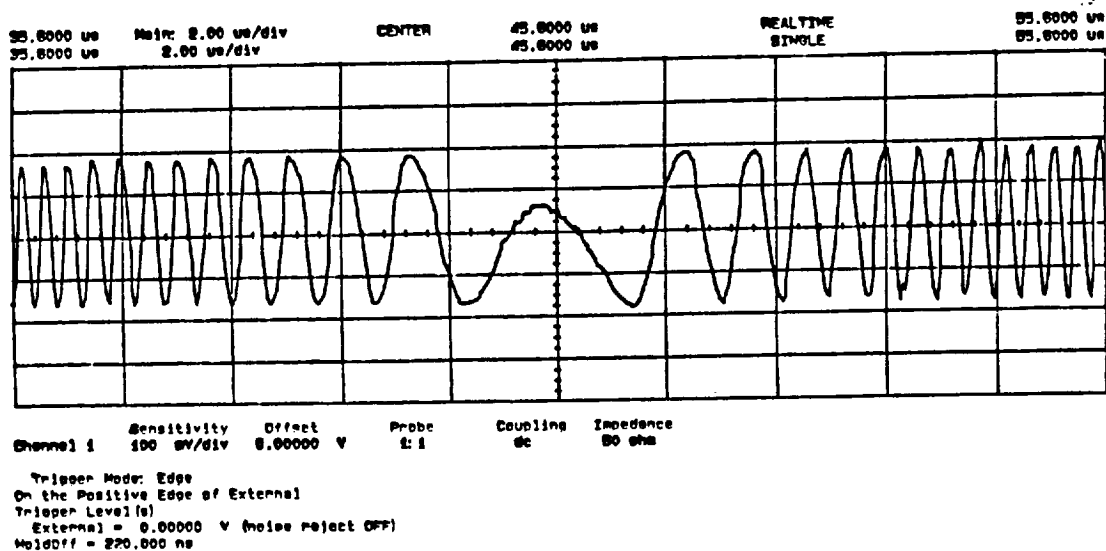


Figure A2-3:- Output Waveform of SSB Modulator

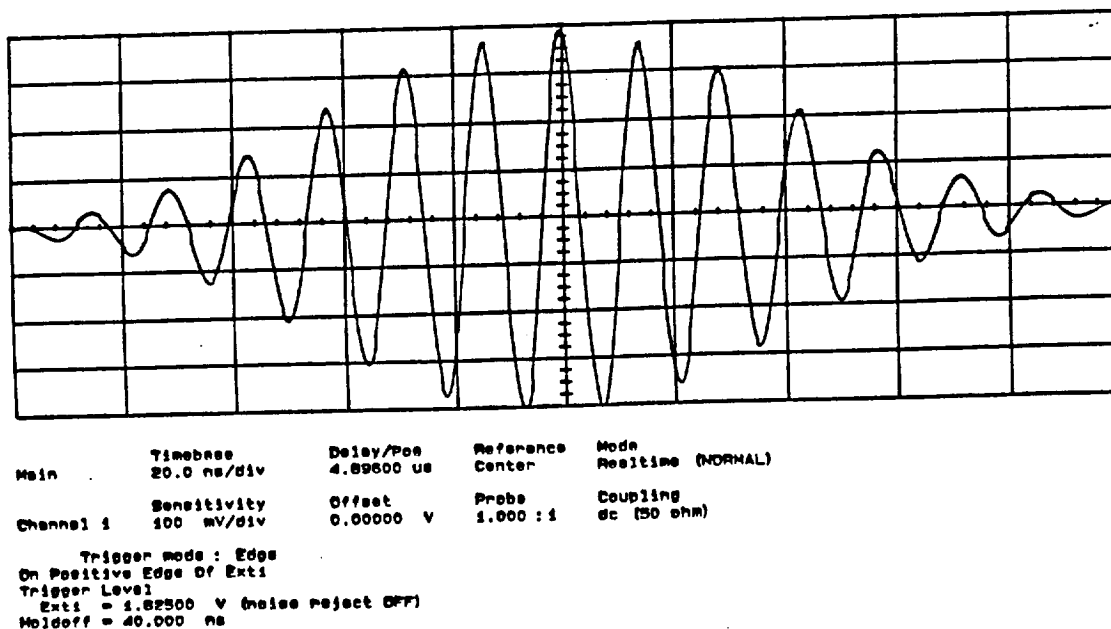
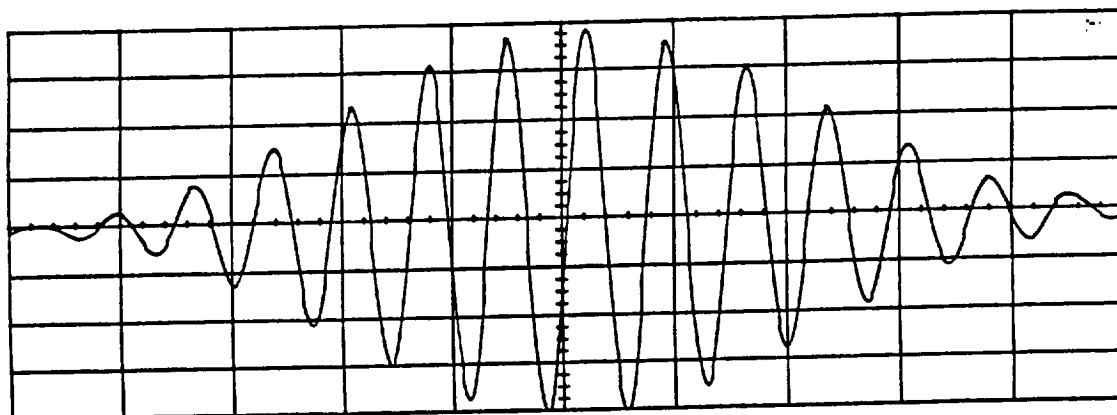


Figure A2-4:- Measured Output Waveform of CMC Transform Processor for $f_0 = 70$ MHz



Main	Timebase	Delay/Pos	Reference	Mode
	20.0 ns/div	4.89600 us	Center	Resetime (NORMAL)
Channel 1	Sensitivity	Offset	Probe	Coupling
	100 mV/div	0.00000 V	1.000 :1	dc (50 ohm)

Trigger mode : Edge
 On Positive Edge Of Ext1
 Trigger Level
 Ext1 = 1.62500 V (noise reject OFF)
 Holdoff = 40.000 ns

Figure A2-5:-Measured Output Waveform of CMC Transform Processor for $f_0 = 70.0015$ MHz

A3. TEMPERATURE EFFECT ON CMC-PROCESSOR

Ambient temperature variations effect the performance of the CMC-Processor. The source of these effects are common, that is due to temperature expansion of the SAW devices. The input and output SAW dispersive filters of the CMC-Processor are made of lithium niobate, LiNbO_3 , crystal, which has a temperature expansion coefficient of 90 PPM/ $^{\circ}\text{C}$. Consequently, as the ambient temperature varies the delay of the filters increases or decreases, so that the length T of the frequency dispersion expands or contracts with varying temperature, resulting in changes of the time frequency slope (chirp slope) of the impulse response of the filter. The latter effect is due to the slope's proportionality to B/T , where B is the filter bandwidth. A change in the chirp slope causes time displacement of the chirp transform output w.r.t. the frame. In addition, effect of ambient temperature variations also causes phase shifts in the carrier of the chirp transform output. This effect, however, is compensated by the carrier tracking circuit of the QPSK demodulator. In what follows, these effects will be analyzed and quantified.

As can be seen from Equation (A1-7), the carrier phase shift is dependent on τ , where

$$\Phi(\omega_s, \tau) = (-\omega_s d) \quad (\text{A3-1})$$

and,

$$\tau = (\omega_s + \omega_1 - \omega_2)/2k + \epsilon \quad (\text{A3-2})$$

At the center of the transform output $\epsilon = 0$, in this case $\tau = \tau_0$. Since τ is effected by the ambient temperature, the carrier phase shift is also effected, but as mentioned earlier the carrier phase tracking circuit will compensate for this change. It is clear from Equation (A3-2) that τ_0 is inversely proportional to k , where $\mu = 2k$ is the chirp slope and $k = \pi B/T$. As T changes due to temperature variations, so will k . Using the system parameters of the Advanced Satellite Communications Receiver, where $B = 32.768 \text{ MHz}$ and $T = 15.625 \mu\text{sec}$, and the temperature coefficient of the SAW material is 90 PPM/ $^{\circ}\text{C}$, the temperature effect is predicted as follows:

Let the ambient temperature (t) range be from -30°C to $+60^{\circ}\text{C}$, hence $\Delta t = -90^{\circ}$ and, w.r.t. $t_a = 25^{\circ}\text{C}$, the temperature variation range is $-55^{\circ}/+35^{\circ}\text{C}$. Therefore, the change in the chirp period, $\Delta T = -.077 \mu\text{sec}/+.049 \mu\text{sec}$ respectively. It can be shown from (A2-7) that the width of the transform output pulse ($\sin x/x$), i.e. null-to-null, is approximately 60 nsec, therefore the temperature effect is significant.

The time displacement of the output pulse is derived from,

$$\tau_0 = (\omega_s - \omega_0)T/2\pi B$$

where the center of the input filter, $\omega_0 = \omega_1 - \omega_2$. The time reference axis is defined at $\omega_s = \omega_0$, where $\tau_0 = 0$.

$$\Delta\tau_0/\Delta T = (\omega_s - \omega_0)/2\pi B$$

$$\therefore \Delta\tau_0 = (\omega_s - \omega_0)\Delta T/2\pi B \quad (\text{A3-3})$$

It is apparent from Equation (A3-3) that $\Delta\tau_0$ is also dependent on the distance of the input signal frequency from ω_0 . This factor has to be taken into account upon designing the temperature tracking circuit. In this analysis, only the extreme case at the edge of the band is considered, that is when $\|\omega_s - \omega_0\|$ is 102.9 Mrad/sec (16.384 MHz). At the extreme low and high temperatures $\Delta\tau_0$ is computed.

From Equation (A3-3), $\Delta\tau_0$ is derived,

$$\Delta\tau_0 = .5\Delta T \quad (\text{A3-4})$$

$$\therefore \Delta\tau_0 = -.0385 \mu\text{sec} \text{ --- } t_a = -30^{\circ}\text{C}$$

$$\Delta\tau_0 = +.0245 \mu\text{sec} \text{ --- } t_a = +60^{\circ}\text{C}$$

Therefore, as t_a varies from -30°C to $+60^{\circ}\text{C}$, for frequencies above and below ω_0 the results are as follows,

For $\omega \geq \omega_0$, $\Delta\tau_0$ is within $-.0385 \mu\text{sec}/+.0245 \mu\text{sec}$, relative to $\Delta\tau_0$ at 25°C .

For $\omega \leq \omega_0$, $\Delta\tau_0$ is within $+.0385 \mu\text{sec}/-.0245 \mu\text{sec}$, relative to $\Delta\tau_0$ at 25°C .

Note that at the center frequency, $\omega_s = \omega_0$, although $\Delta\tau_0 = 0$ the transform output time reference axis is shifted, with respect to the chirp generator timebase, when the ambient temperature changes. This time shift is due to the basic time delay ($\tau_r \mu\text{sec}$ at

25°C) of the SAW filter, which also varies with temperature directly proportional to the temperature expansion coefficient of the SAW crystal.

In the implementation of the temperature compensation and tracking circuit, a CW reference signal could be injected into the CMC-Processor and monitored at the output. The time shift due to ambient temperature variations monitored at the output of the CMC-Processor would include $\Delta\tau_0$ and $\Delta\tau_r$. The latter is common for all input frequencies, therefore, at any other frequency a correction has to be made to account for $\Delta\tau_r$. In case of the Advanced Satellite Communications Receiver, a correction factor (F_T) can be predetermined based on the system parameters.

Let ω_{sr} be the reference signal frequency, τ_r the basic delay at the center frequency ω_0 and $t_a = 25^\circ\text{C}$, and C the temperature expansion coefficient of the SAW crystal. Hence, at an ambient temperature of t_1 , the reference signal at the CMC-Processor output is delayed (w.r.t. the chirp transform frame period T) by τ_{tr} , where

$$\tau_{tr} = \tau_r(1 + \Delta t.C) + (\omega_{sr} - \omega_0)(1 + \Delta t.C)T/2\pi B \quad (\text{A3-5})$$

The first term in Equation (A3-5) is due to the change in basic delay (temperature expansion). The second term is due to the change in time displacement of the output transform pulse w.r.t. the chirp generator timebase or frame (caused by a change in chirp slope).

The delay at ω_s is,

$$\tau_{ts} = \tau_r(1 + \Delta t.C) + (\omega_s - \omega_0)(1 + \Delta t.C)T/2\pi B \quad (\text{A3-6})$$

$$\therefore \Delta\tau = \tau_{ts} - \tau_{tr} = (\omega_s - \omega_{sr})(1 + \Delta t.C)T/2\pi B \quad (\text{A3-7})$$

From Equations (A3-5) and (A3-7), $\Delta\tau/\tau_{tr}$ is derived.

$$\Delta\tau/\tau_{tr} = [(\omega_s - \omega_{sr})T/2\pi B] / [\tau_r + (\omega_s - \omega_0)T/2\pi B] \quad (\text{A3-8})$$

From Equation (A3-7), $\tau_{ts} = \tau_{tr} + \Delta\tau$, this can be rewritten as

$$\tau_{ts} = (1 + \Delta\tau/\tau_{tr})\tau_{tr} \quad (\text{A3-9})$$

Consequently, from Equation (A3-9) the correction factor (F_T) for τ_{ts} is obtained.

$$F_T = 1 + \Delta\tau/\tau_{tr} \quad (\text{A3-10})$$

Where $\Delta\tau/\tau_{tr}$ is given by Equation (A3-8).

Since for a given channel of the Advanced Satellite Communications Receiver, containing a CMC-Processor, each variable in Equation (A3-8) is known a priori, the correction factor for temperature compensation and tracking can be computed and taken into account. In practice, the development of an automatic tracking circuit is recommended.